An Implementation of 9-Level MLI using IPD-Topology for Harmonic Reduction

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ABSTRACT
Multi Level Inverters (MLI) are today used in medium and large power applications. There are three major topologies of multilevel inverters; they are capacitor clamped, diode camped and cascaded. During this paper implement the nine-level asymmetric cascaded multilevel inverter with IM for various kinds of level-shifted PWM techniques in Matlab Simulink. As the number of levels will increase, the synthesized output waveform has more steps that produces a staircase wave that approaches the required waveform. Also, as more steps are added to the waveform, the harmonic distortion of the output wave decreases, approaching zero as the number of levels will increase. As the number of levels will increase, the voltage that can be spanned by connecting devices serial also increases.

Keywords— Inverter, Multilevel Inverter, Power Electronics, PWM, AC, DC

I. INTRODUCTION
In recent years, multilevel inverters have received more attention in industrial applications, such as motor drives, Static VAR Compensators (STATCOMs), Flexible AC Transmission System (FACTS), high voltage direct current lines, electrical drives and renewable energy systems [2].

Compared to the traditional two level voltage source inverters, the stepwise output voltage is the major advantage of multilevel inverters. This advantage results in higher power and needlessness of a transformer at distribution voltage level, thereby reducing the costs. Multilevel inverters are generally divided into three configurations: diode-clamped, flying-capacitor, and cascaded H-bridge multilevel inverters [3]. Among these inverter topologies, cascaded multilevel inverter reaches the higher output voltage and power levels and the higher reliability due to its modular structure. Cascaded multilevel inverters are based on a series connection of several single phase full bridge inverters. This structure is capable of reaching medium output voltage levels using only standard low voltage components [4].

Typically, it is necessary to connect three to ten inverters in series to reach the required output voltage. These converters also feature a high modularity degree because each inverter can be seen as a module with similar circuit topology, control structure, and modulation. Therefore, in the case of a fault in one of these modules, it is possible to replace it quickly and easily. Moreover, with an appropriated control strategy, it is possible to bypass the faulty module without stopping the load, bringing an almost continuous overall availability.

II. LITERATURE SURVEY
Summary- In general, the inverter output voltage must be sinusoidal. However, the waveforms of the inverters practical non-sinusoidal and contain certain harmonics. For low and medium power applications, square wave or quasi-square wave may be acceptable, but for high power applications, low distorted sinusoidal waveforms are required. By number of levels in the UPS by increasing the output voltage has several steps generating a form of stairs, which reduces harmonic distortion. Emerges need a multi-level inverter. In this cascade research work multilevel inverter with selective removal of Pulse Width Modulation harmonics (SHE-PWM) technique is implemented. The SHE-PWM problem is to solve the non-linear transcendental equations that are used to determine the switching angles. Here the evolutionary algorithm based on natural selection is proposed to solve the equations that reduce the computational load resulting from the faster convergence. The main benefits are reduced total harmonic distortion and low switching frequency. To validate the results of calculation for the switching angles, a simulation is performed in the MATLAB / Simulink software tool for a level 7 cascade H-bridge inverter. [1]


Summary- Multilevel inverters have been widely used in applications in medium and high voltage. Selective Harmonic Elimination for voltage waveform generated by the staircase multilevel inverter has been widely studied in the last decade. Most methods published on this subject were based on solving multivariate groups of high order polynomial equation from the Fourier series expansion. This research presents a different approach, which is based on criteria of equal and harmonic injection area. With the proposed method, regardless of the number of voltage levels are involved, only four simple equations are needed. The results of a case study, with a maximum of five switching angles show that the proposed method can be used to achieve excellent removal performance of the harmonics of the modulation index range of at least 0, 2 to 0.9. To demonstrate the adaptability of the proposed method for waveforms with a high number of switching angles, experimental results on a 1-MVA 6000 V-17 level cascaded multilevel inverter are also presented to the end of this research. [2]


Summary- In this research, an optimization technique is proposed to calculate the switching angles to the fundamental frequency of switch system by solving nonlinear transcendental equations (known as selective harmonic elimination equations), thus eliminating certain harmonics predominating lower order, and at the same time, control over the magnitude of the output voltage of a multilevel inverter is reached. Since these equations are nonlinear transcendental in nature, there may be a simple, multiple or even for a particular value of a modulation index. The proposed scheme is implemented so that all possible solutions are obtained without knowing the proper initial estimate solutions. Moreover, this technique is suitable for the high level of multilevel inverters where other existing methods fail to calculate switching angles due to more computational load. For values of modulation indices for which there are many solutions, the solutions that produce less THD in the output voltage is selected. A significant decrease DHT is obtained by considering several sets of solutions instead of taking a single set of solution. Calculation results are displayed graphically for better understanding and proving the effectiveness of the method. An experimental 11-level multi-level cascade inverter is used to validate the results of calculation. [6]

III. PROPOSED METHODOLOGY

During this chapter implement the nine-level asymmetric cascaded multilevel inverter with IM for various kinds of level-shifted PWM techniques in Matlab Simulink. As the number of levels will increase, the synthesized output waveform has more steps that produces a staircase wave that approaches the required waveform. Also, as more steps are added to the waveform, the harmonic distortion of the output wave decreases, approaching zero as the number of levels will increase. As the number of levels will increase, the voltage that can be spanned by connecting devices serial also increases.

The output voltage of the MLI has several levels synthesized from many dc voltage sources, the quality of the output voltage is improved as the no of voltage levels increase, therefore total harmonic distortions and therefore the quantity of output filter can be reduces.

IV. PROPOSED SYSETEM

4.1 Block Diagram of Proposed Work

In case of 9 level Asymmetric Cascaded MLI three DC sources are used having 2 same and third different and 12 power switches are used. The Asymmetric Multilevel Inverter increases the number of levels in the output and reduces the number of input DC sources required. IGBT is used as semiconductor switch for designing the inverter circuit. It has the high power rating, less conduction loss and less switching loss. These topology uses level-shifted multi carrier based new PWM method, used to produce a 9-level output voltage.

![Figure 2: Proposed block diagram of 9-levels Hybrid Cascaded Multilevel Inverter](image-url)
4.2 SCHEMATIC DESCRIPTION OF THE SYSTEM

4.2.1 Simulation Diagram

The Simulink model of 9-level multilevel inverter implemented in Matlab-Simulink is shown in Figure 3. It is basically a Cascaded H-bridge type of Multilevel Inverter.

Here the used DC source is Asymmetrical type. Asymmetrical source defines that it has different value of DC sources used in an Inverter. For 9-level inverter the DC sources are 100V, 200V, and 100V respectively. The Simulink model for 9-level multilevel inverter shown in figure 3.

![Simulink model of 9 level with IM](image)

Figure 3: Simulink model of 9 level with IM

4.2.2 Working and Analysis

Working of this inverter is nothing but how we make power switches (IGBTs) ON and OFF as per voltage level desired. We have generated switching pulses to obtain staircase output voltage which resembles nearly equal to sine wave. For different switching angles the power circuit behaves differently producing different waveforms. In this topology, we have generated 9 voltage levels as 0, 100V, 200V, 300V and 400V. The circuit working for each level is described below:

A. For 0 voltage level

Since S1 and S3 are ON or all power switches are OFF, the current will cancelled out in the bridge and hence it gives 0 V voltage level.

B. For 100V voltage level

Since S1, S4, S5, S6, S10 & S12 are ON and remaining switches are OFF, the voltage across load will give 100V level.

C. For 200V voltage level

Since S1, S4, S5, S6, S10 & S12 are ON and remaining switches are OFF, the voltage across load will give 200V level.

D. For 300V voltage level

Since S1, S2, S5, S6, S10 & S12 are ON and remaining switches are OFF, the voltage across load will give 300V level.

E. For 400V voltage level

Since S1, S2, S5, S6, S9 & S10 are ON and remaining switches are OFF, the voltage across load will give 400V level.

F. For 0V voltage level

Since S1 and S3 are ON or all power switches are OFF, the current will cancelled out in the bridge and hence it gives 0 V voltage level.

G. For -100V voltage level

Since S3, S4, S6, S8, S10, and S12 are ON and remaining switches are OFF, the voltages across load will give -100V level.

H. For -200V voltage level

Since S2, S4, S7, S8, S10, and S12 are ON and remaining switches are OFF, the voltages across load will give -200V level.

I. For 300V voltage level

Since S3, S4, S7, S8, S10, & S12 are ON and remaining switches are OFF, the voltages across load will give -300V level.

J. For -400V voltage level

Since S3, S4, S7, S8, S11, & S12 are ON and remaining switches are OFF, the voltages across load will give -400V level.

For detail operation of new topology can also be understand by analyzing table 1 which is given below. Here 0 means switches are OFF and 1 means switches are ON.

<table>
<thead>
<tr>
<th>Output Voltage</th>
<th>400V</th>
<th>300V</th>
<th>200V</th>
<th>100V</th>
<th>0V</th>
</tr>
</thead>
<tbody>
<tr>
<td>S1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>S2</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>S3</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>S4</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>S5</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>S6</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>S7</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>S8</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>S9</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>S10</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>S11</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>S12</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

Table 4.1: Switching pattern for asymmetrical cascaded nine level inverter

<table>
<thead>
<tr>
<th>System Parameters</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reference frequency</td>
<td>50 Hz</td>
</tr>
<tr>
<td>Carrier frequency</td>
<td>1.2K Hz</td>
</tr>
<tr>
<td>Load resistance</td>
<td>1Ω</td>
</tr>
<tr>
<td>Load inductance</td>
<td>1 mH</td>
</tr>
<tr>
<td>DC Sources</td>
<td>100V, 200V, 300V</td>
</tr>
</tbody>
</table>

Table 4.2: System parameters for 9-level Inverter
V. SIMULATION AND RESULT

This section shows the comparative study of output voltage of 9-level asymmetrical cascaded multilevel inverters cascaded is compared for the PD, POD, APOD techniques, and it also shows the THD profile and performance of the circuit with IM for three PWM techniques, and also the compare all result with 7-level MLI.

Cascaded multi-level inverter shows the lowest THD profile without any type of filter and also any type of dependency of inductor and capacitor used for smooth the current wave form and due to less number of switching devices gate firing circuit also reduced that’s why total cost and performance has been increased.

5.1 SIMULATION RESULT OF (9-LEVEL) ACMLI WITH IM USING IPD-CLSPWM

VI. RESULT COMPRESSION

In this of the compare the result of proposed method 9-level with 7 level MLI. In the below figure 7 shows the output of 7 level multi level inverter. In the genetic cascaded multilevel inverter with Selective Harmonic Elimination Pulse Width Modulation (SHE-PWM) technique is implemented. The problem of SHE-PWM is to solve the nonlinear transcendental equations which are used to determine switching angles.

6.5 RESULT

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The total harmonic distortion of the 7 level genetic algorithm is near about 11.33%. In the proposed 9-level asymmetric (9-level) MLI using IPD-CLSPWM THD is shown in below figure 8.

![THD of Proposed 9-Level Inverter](image)

Fig 8. Show the THD of Proposed 9-Level Inverter

**VII. CONCLUSION**

In this work, the multicarrier pulse width modulation (PWM) techniques for 9-level have been presented. Performance factor like total harmonic distortion (THD) of the output voltage of asymmetric cascade multi-level inverter (CMLI) have been evaluated, presented and analyzed. The total harmonic distortion (THD) of the output voltage of unbalanced cascade multi-level inverter (CMLI) is studied under different techniques such as IPD, POD & APOD, compare for seven and nine level multi-level inverter (MLI) and less total harmonic distortion (THD) is observed for APOD techniques for 7-level and IPD techniques best for 9-level multi-level inverter (MLI). Therefore, it concluded that the 9-level cascade multi-level inverter (CMLI) provide a lower percentage total harmonic distortion (THD) as compared to 7-level multi-level inverter (MLI). The harmonic distortions present in the output voltage waveforms were experiential and calculate from side to side Fast Fourier Transform (FFT) analysis tool in Matlab and Simulink.

The proposed inverter has been operated by only three control schemes, namely IPD, POD and APOD PWM schemes. Applying the improved switching techniques can still improve the output quality. So potential of proposed version could be explored by adopting different switching techniques. The proposed version of CMI is only adopted for harmonic reduction applications. In fact the merits of CMI can be used to build for photovoltaic/grid connected systems. So it can extend to multiple applications like STATCOM, SSSC and UPQC etc.

**REFERENCES**


