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# Design & Implementation of Vedic Multiplier on FPGA

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**ABSTRACT**

**This paper projected the design of high speed Vedic Multiplier by the techniques of Ancient Indian Vedic Mathematics that have been customized to get betterperformance. Vedic Mathematics be the ancient scheme of mathematics which has a sole technique of calculations based on 16 Sutras. The work has proved the effectiveness of UrdhvaTriyagbhyam– Vedic method for multiplication which strikes a distinctionduring the real process of multiplication itself. Urdhvatiryakbhyam Sutra is most resourceful Sutra, giving minimum delay for multiplication of all types of numbers. Further, the Verilog HDL coding of Urdhvatiryakbhyam Sutra for 16x16 bits multiplication and their FPGA implementation by Xilinx10.1 and MODELSIM 6.4a software's on Spartan 3E kit have been done. The synthesis results show that the path delay for calculating the product of 16x16 bits is24.906 ns. When Vedic Multiplier is compared with classical Vedic multipliers it is advantageous in each aspect. The study reveals that Vedic multiplier has least path delay when compared with its other peer existing multipliers structures.**

***Keywords***------- Vedic Mathematics, Vedic Multiplier, Urdhava Tiryakbhyam Sutra

## I. INTRODUCTION

Multiplication is an essential basic function in arithmetic operations. The multiplication dominates the execution time of most DSP algorithms, so there should be a need of high speed multipliers. Multiplication time is still the leading factor for determining the instruction cycle time of a DSP chip .The demand for high speed processing is increasing as a result of expanding computer and signal processing applications. Higher throughput arithmetic time signal and operations are significant to attain the desired performance in many real- image processing applications. One of the key arithmetic operations in such applications is multiplication and the advance of fast multiplier circuit has been a subject of interest over years. Since multiplication dominates the execution time of most DSP algorithms, so there is a need of high speed multipliers. Higher throughput arithmetic operations are important to achieve the desired performance in many real-time signal.For many Digital Signal Processing (DSP) applications such as convolution, filtering and in ALU of microprocessors and image processing applications reducing the time delay is important requirement.[1]Vedic mathematics is the name which isgiven to the ancient Indian system of mathematics that was rediscovered in near the beginning of twentieth century.

Vedic mathematics is mostly based on sixteen principles or word-formulae which are termed as Sutras. A simple digital multiplier (referred henceforth as Vedic multiplier) architecture based on the UrdhvaTriyakbhyam (Vertically and Cross wise) Sutra is presented. This Sutra was usually used in ancient India for the multiplication of two decimal numbers in comparatively less time. In this paper, after a gentle introduction of this Sutra, it is apply to the binary number system to make it valuable in the digital hardware.[2]This paper shows a new insight into the multiplication process. The projected approach in this method is based on the Vedic method of multiplication. The Vedic method of multiplication is based on the sutra "vertically and crosswise". Let us wish to multiply 32 by 44. We multiply vertically 2x4=8. Then we multiply crosswise and add the two results: 3x4+4x2=20, so put down 0 and carry 2. Finally we multiply vertically 3x4=12 and add the carried 2 = 14.Result = 1,408.

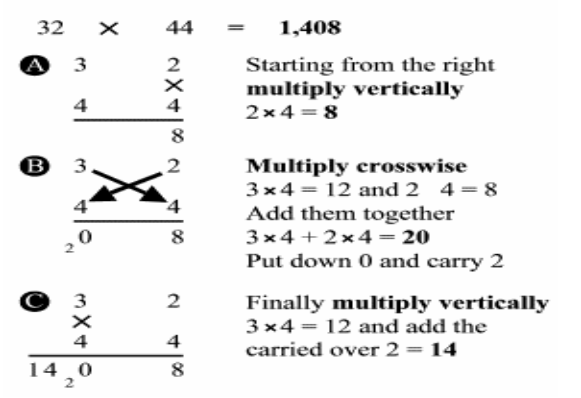


Fig 1: Example of Multiplication By Vedic Method [2].

## II. VEDIC MATHEMATICS (VM)

Vedic mathematics isa part of four Vedas. It is a part of Sthapatya- Veda (book on civil engineering ), which is an upa-veda (supplement) of Atharva Veda. It gives description of several mathematical terms including arithmetic, geometry (plane, co-ordinate), trigonometry, quadratic equations and factorization. His Holiness JagadguruShankaracharyaBharati Krishna Teerthaji Maharaja (1884-1960) comprised all this work together and gave its mathematical description while discussing it for different applications. Swamhiji constructed 16 sutras (formulae) and 16 Upa sutras (sub formulae) after wide research in Atharva Veda.

The very word „Veda‟has the derivational meaning i.e. the source and unlimited storehouse of all knowledge. Vedic mathematics is the name given to the ancient system of mathematics or, to be present a unique technique of calculations based on simple rules and principles with which many mathematical problems can be solved be it arithmetic, algebra, geometry or trigonometry. The system is based on 16 Vedic sutras, which are really word formulae describing usual ways of solving a whole collection of mathematical problems. The magnificence of Vedic mathematics lies in the fact that it reduces the otherwise cumbersome-looking calculations in conventional mathematics to a very simple one. This is so because the Vedic formulae are claimed to be based on the natural principles on which the human mind works. This is a very exciting field and presents some effectual algorithms which can be applied to various branches of engineering such as computing and digital signal processing.

A. These Sutras along with their brief meanings are enlisted below alphabetically:

1. (Anurupye) Shunyamanyat – If one is in ratio, the other is zero.
2. Chalana-Kalanabyham – Differences and Similarities.
3. EkadhikinaPurvena – By one more than the previous One.
4. EkanyunenaPurvena – By one less than the previous one.
5. Gunakasamuchyah – The factors of the sum is equal to the sum of the factors.
6. Gunitasamuchyah – The product of the sum is equal to the sum of the product.
7. NikhilamNavatashcaramamDashatah – All from 9 and last from 10.
8. ParaavartyaYojayet – Transpose and adjust.
9. Puranapuranabyham – By the completion or noncompletion.
10. Sankalana- vyavakalanabhyam – By addition and by subtraction.
11. ShesanyankenaCharamena – The remainders by the last digit.
12. ShunyamSaamyasamuccaye – When the sum is the same that sum is zero.
13. Sopaantyadvayamantyam – The ultimate and twice the penultimate.
14. Urdhva-tiryagbhyam – Vertically and crosswise.
15. Vyashtisamanstih – Part and Whole.
16. Yaavadunam – Whatever the extent of its deficiency.

These methods and facts can be directly applied to trigonometry, plain and spherical geometry, conics, calculus (both differential and integral), and applied mathematics of various kinds. As mentioned earlier, all these Sutras were reconstructed from ancient Vedic texts early in the last century.

## III. URDHVATIRYAGBHYAM SUTRA

The „UrdhvaTiryagbhyam‟ Sutra [] is a common multiplication formula applicable to all cases of multiplication. „Urdhva‟ and „Tiryagbhyam‟ words are derived from Sanskrit literature. „Urdhva‟ means “Vertically” and „Tiryagbhyam‟ means “crosswise”. To illustrate thismultiplication idea, suppose the multiplication oftwo decimal numbers (5498 × 2314). The conventional methods already know to us will require 16 multiplicationsand 15 additions [6].An alternative method of multiplication using Urdhva-Tiryakbhyam Sutra is shown in Fig. 2. The numbers which are multiplied are written on two consecutive sides of the square as shown in the figure.The square is separated into rows andcolumns where each row/column corresponds to one of the digit of either a multiplier or a multiplicand. Thus, each digit of the multiplier has a small box common to a digit of the multiplicand. These small boxes are divided into two halves by the crosswise lines. Each digit of the multiplier is then separately multiplied with every digit of the multiplicand and the two-digit product is written in the common box. All the digits lying on a crosswise dotted line are added to the previous carry. The least significant digit of theobtain number acts as the result digit and the rest as the carry for the next step. Carry for the first step (i.e., the dotted line on the extreme right side) is taken to be zero.

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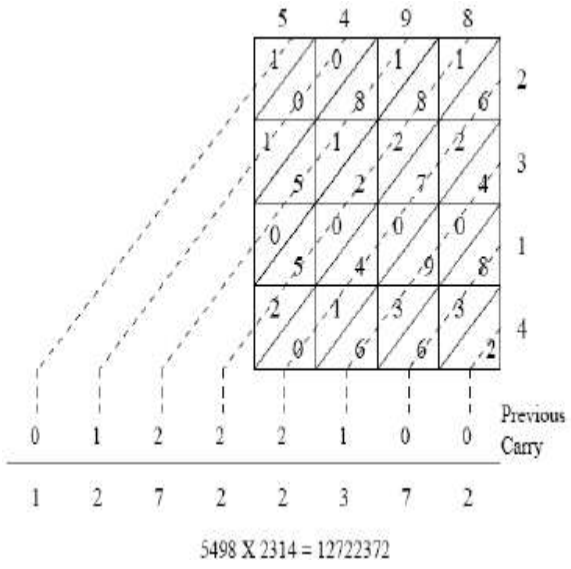


Fig. 2 Multiplication of two large integers

Let us consider the multiplication of two 2-bit binary numbers a1a0 and b1b0. Firstly, the least significant bits are multiplied which gives the least significant bit of the final product (vertical). Then, the LSB of the multiplicand is multiplied with the next higher bit of the multiplier and added with, the product of LSB of multiplier and next higher bit of the multiplicand (crosswise). The sum gives second bit of the final product and the carry is added with the partial product obtained by multiplying the most significant bits to give the sum and carry. The sum is the third consequent bit and carry becomes the fourth bit of the final product.The 2×2 Vedic multiplier module is then used to implement higher level multipliers (4×4 multiplier, 8×8 multiplier, 16×16 multiplier).

# IV. 16X16 VEDIC MULTIPLIER MODULE

The 16x16 bit Vedic multiplier module as shown in the block diagram in Figure 3 can be easily implemented by using four 8x8 bit Vedic multiplier modules as discussed in the previous section Let's analyze 16x16 multiplications, say A= a15 a14 a13 a12 a11 a10 a9 a8 a7 a6 a5 a4 a3 a2 a1 a0 and B= b15 b14 b13 b12 b11 b10 b9 b8 b7 b6 b5b4 b3 b2 b1b0. The output line for the multiplication result will be of 32 bits as – s31 s30 s29 s28 s27 s26 s25 s24 s23 s22 s21 s20 s19 s18 s17 s16 s15 s14 s13 s12 s11 s10 s9 s8 s7 s6bs5s4 s3 s2 s1 s0.

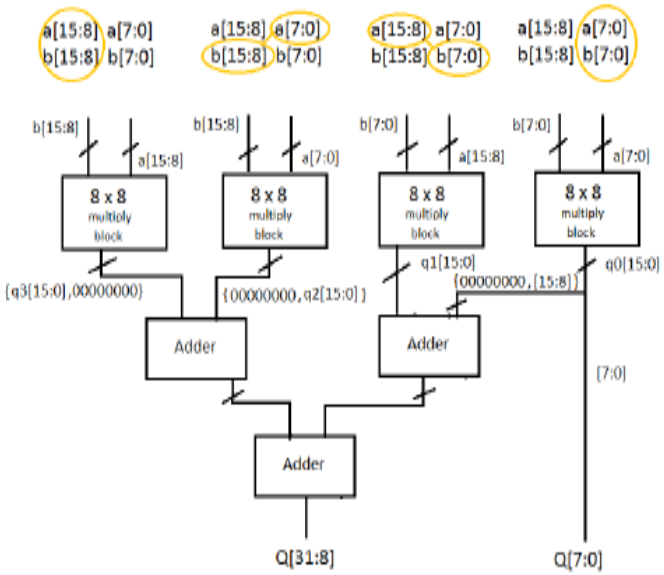


Fig. 3 Block Diagram of 16x16 bit Vedic Multiplier

The 32 bit product can be written as: Using the fundamental of Vedic multiplication, taking eight bits at a time and using 8 bit multiplier block we can perform the multiplication. The outputs of 8x8 bit multipliers are added accordingly to obtain the final product. Here total three Adders are required as shown in Fig. 3.

# V. IMPLEMENTATION OF VEDIC MULTIPLIER

The proposed Vedic multiplications were implemented using Xilinx FPGA Spartan 3E board. Simulation results are verified using Xilinx 10.1 and MODELSIM 6.4a software's. The simulation results for 16x16 Vedic Multiplier is shown in figure 4.
Simulation Results:

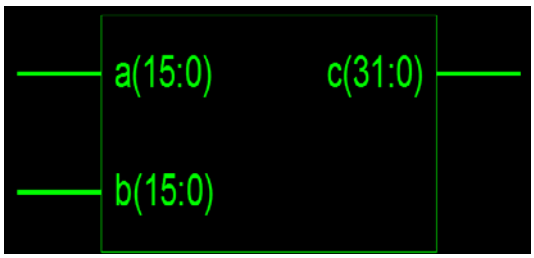


Fig.4(a): 16x16 Vedic Multiplier RTL schemantic1

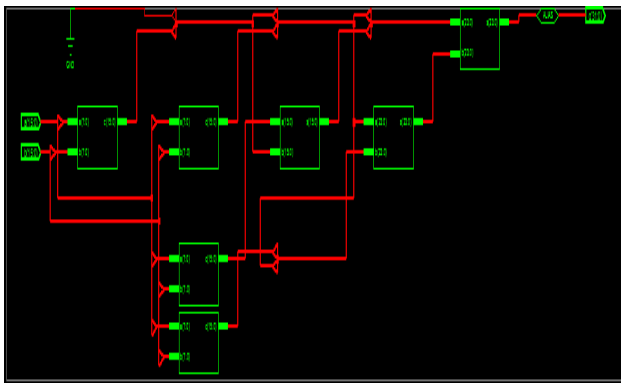

Fig 4(b): 16x16 Vedic Multiplier RTL schemantic2

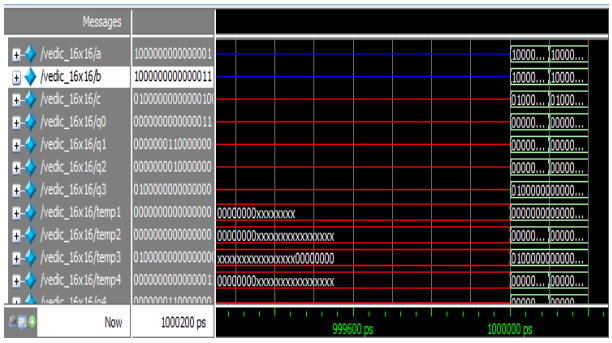


Fig 4(c):Output Waveform of 16 X 16 Vedic Multiplier

***Device Utilization Summary:***

| | |
|---|---|
| **Project File:** | 2bit.ise |
| **Module Name:** | vedic_16x16 |
| **Target Device:** | xc3s100e-5tq144 |
| **Product Version:** | ISE 10.1 - Foundation Simulator |
| **Design Goal:** | Balanced |
| **Design Strategy:** | Xilinx Default (unlocked) |

**Device Utilization Summary**

| Logic Utilization | Used | Available | Utilization |
|---|---|---|---|
| Number of 4 input LUTs | 534 | 1,920 | 27% |
| **Logic Distribution** | | | |
| Number of occupied Slices | 301 | 960 | 31% |
| Number of Slices containing only related logic | 301 | 301 | 100% |
| Number of Slices containing unrelated logic | 0 | 301 | 0% |
| **Total Number of 4 input LUTs** | 577 | 1,920 | 30% |
| Number used as logic | 534 | | |
| Number used as a route-thru | 43 | | |
| Number of bonded IOBs | 64 | 108 | 59% |

The path delay for 16x16 Vedic multiplier was found to be 24.906 ns. The timing delays arefound that tells the time taken by a specific multiplier forperforming its task of multiplication.

## VI. CONCLUSION

When Vedic Multiplier is compared with classical Vedic Multipliers it is advantageous in every aspect. The study reveals that Vedic multiplier has least path delay when compared with other peer existing multipliers.I have synthesized 16 X 16 Vedic Multiplier using verilog on ISE Xilinx10.1 and simulated using MODELSIM 6.4a. Results show that 16 X 16 Vedic Multiplier uses No. Of slices-301, No. Of 4 inputs LUTs -534, No. Of IOBs -64 and also the delay exerted by16 X 16 Vedic Multiplier is 24.906 ns.Delay exerted by above mentioned multiplier is less when compared with the classical Vedic Multipliers which is 25.083 ns using VHDL and the simulation results are obtained on MODELSIM. Hence while comparing 16 X 16 Vedic Multiplier with classical Vedic Multipliers which uses Carry Save Adder which increases the speed of addition in partial product generated during multiplication in terms of delay, even then it is faster. Hence it is useful in industries.

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