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# Implementation of Efficient 5:3 & 7:3 Compressors for High Speed and Low-Power Operations

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**ABSTRACT**

**This paper demonstrate high speed and low-power compressors (5:3 and 7:3) for efficient parallel multipliers in Digital Signal Processing (DSP), simulated with Tanner EDA Tools. This is achieved by rapid critical path reduction than the conventional compressors. Though conventional 5:3 compressor need four steps to reduce bits from 5 to 3, the used 5:3 requires only 2 steps. For the investigation of overall performance of the simulated compressors in terms of delay and energy consumption; power, delay and power delay product (PDP) of the compressors are being analyzed.**

***Keywords***-- tanner EDA tools, compressors, ECRL, GDI, 14T, TG

## I. INTRODUCTION

Fast arithmetic computation cells (adders, multipliers etc.) are the widely used circuit in VLSI systems. These are generally composed three subsections, viz., partial product generation, partial product accumulation and then addition. In partial product generation booth encoding is used to reduce the partial product, while in the partial product accumulation Carry Save Adder (CSA) is used to again reduce the partial product. The last function is used to carry propagate adder, such as CLA adder and CSA. One of the better options is to use compressors (5:3 or 7:3) by which we can reduce the partial product and final carry with minimum gate delay and low power loss.

## II. IMPLEMENTED LOGICS

### *1. Conventional full adder*

Regular CMOS structure based static CMOS standard full adder gives full-swing output and better driving capability [1]. However, the presence of the PMOS block having lesser mobility than the NMOS block in static CMOS circuits is a major drawback. Thus to achieve desired performance the PMOS and NMOS block should be sized up properly. The circuit diagram of a conventional full adder is shown in Figure 1.

### *2. Gate Diffusion Input (GDI) full adder*

The circuit of GDI [2] based full adders shown in Figure 2, generates the sum bit from the output of the second stage of XOR circuit and carry bit by multiplexed B and *C* controlled by (A XNOR B). Thus in a GDI cell 2 extra input pins are used to make it more flexible and power efficient than conventional CMOS design [3], without large transistor count. The major drawback of a GDI cell is that it requires twin-well CMOS and so it will be more expensive to realize it. However if standard p-well CMOS process is only used, lack of driving capability makes it more difficult and expensive to be realized [4].

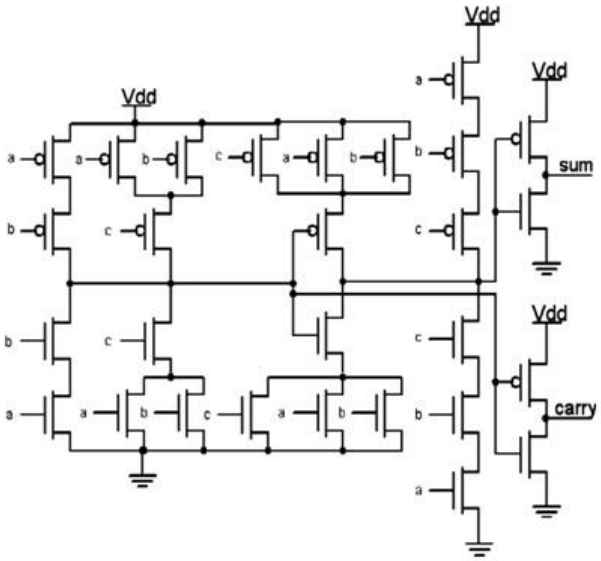


**Figure 1: Conventional full adder**

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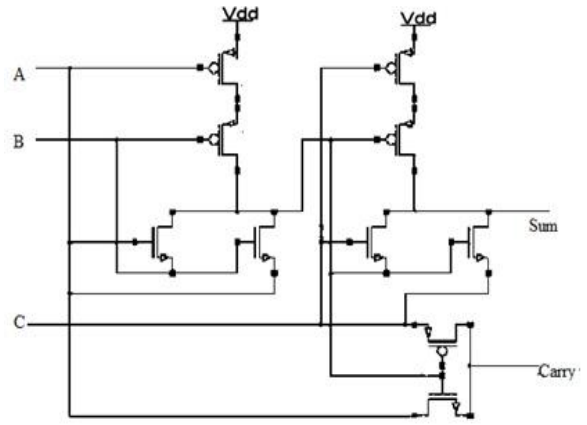


**Figure 2: GDI full adder**

### *3. Transmission Gate (TG) full adder*

These are inherently low power consuming pass-transistor logic circuit, simpler than the conventional adder, but there is a drawback of low driving capability. It is controlled by complementary control signals developed by connecting one NMOS and one PMOS transistor in parallel, 2 inverters followed by 2 TG, acting as 8-T XOR followed by 8-T XNOR module, as shown in Figure 3. The circuit produces proper polarity buffered outputs for both sum and carry bits [5].

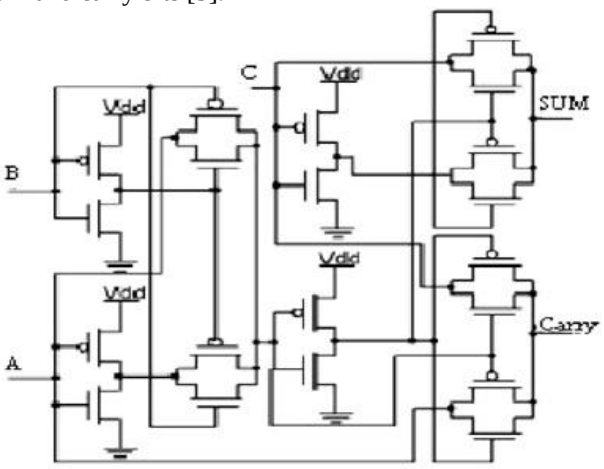


**Figure 3: TG full adder**

### *4. Efficient Charge Recovery Logic (ECRL) full adder*

ECRL [6] structure based on cross-coupled PMOS transistor and NMOS transistors is similar to Cascode Voltage Switch Logic (CVSL) with differential signal, shown in Figure 4 and the ECRL full adder circuit is shown in the Figure 5. For the recovery and recycle the supplied energy, an AC supply power is used for ECRL gates. Both outputs are so generated that irrespective of the signal input, a constant load capacitance is derived by the power clock generator. For the presence of the cross-coupled PMOS transistors in both pre-charge and recovery phases total output swing is obtained, but due to the threshold voltage of the PMOS transistors, the circuits suffer from the non-adiabatic loss in both the phases.

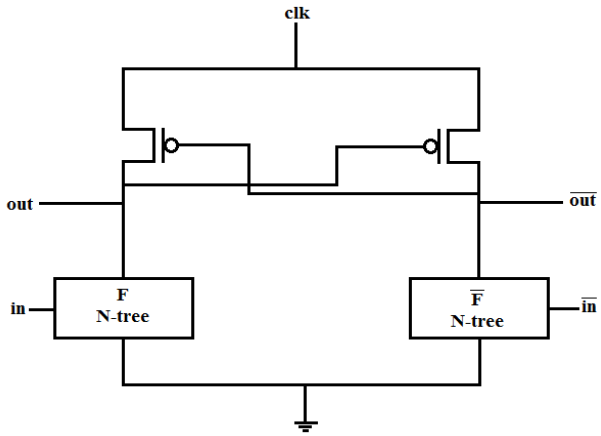


**Figure 4: ECRL logic structure**

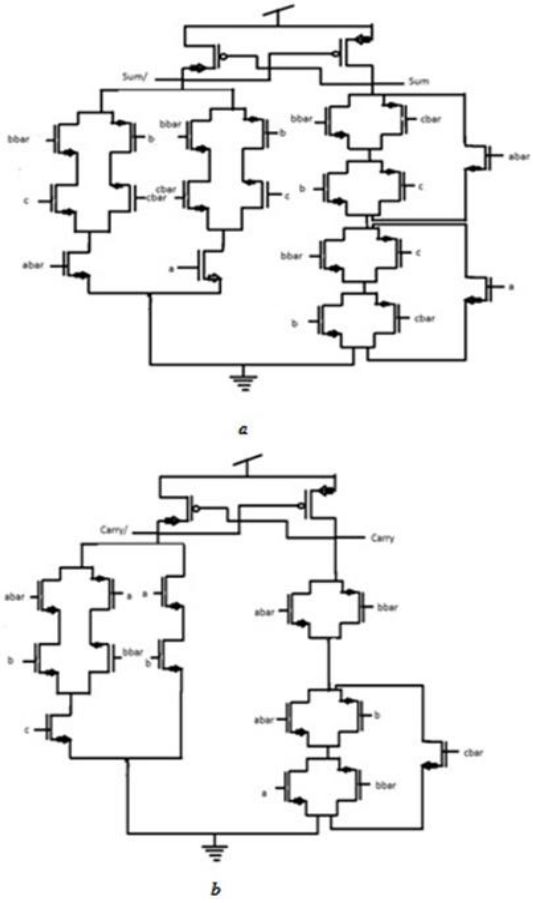


**Figure 5: ECRL full adder**

### *5. 14T full adder*

14T full adder, shown in Figure 6 contains a 4-transistor XOR gate with pass transistor logic, an inverter and TG based MUX design for SUM and CARRY outputs [7]. This circuit with 4T XOR, inverted to generate XNOR

in the next stage and they generate simultaneously the SUM and CARRY outputs. The signals C and C bar are multiplexed and can be controlled either by (AB) or (A⊗B). Similarly, CARRY can be calculated by multiplexed A and C, controlled by (AB). It is a faster adder with a simpler circuit compared to the conventional one [8, 9].

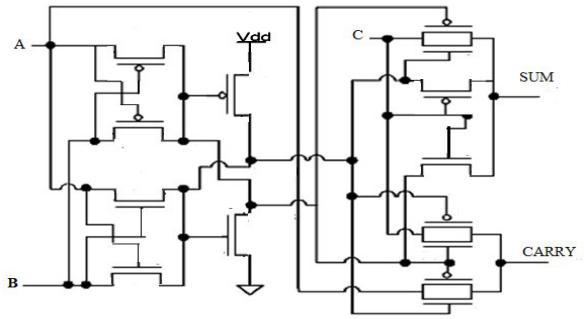


**Figure 6: 14 T full adder**

## III. COMPRESSOR ARCHITECTURE

The two types of compressors we have designed are: i) 5:3 Compressor and ii) 7:3 Compressor.

***1. 5:3 Compressor***

A 5:3 compressor comprises with a combinational logic circuit having 5 inputs and 3 outputs. It accepts a5 bit input string as input, and produces its sum as output. The conventional architecture of a 5:3 compressor is based on the extended design of a conventional 4:2 compressor. Figure 7 shows the architecture of a conventional 5:3 compressor. Table I shows the number of different parameters used in Tanner EDA for circuit connections of the 5:3 compressor using different logics.

***2. 7:3 Compressor***

A 7-3 compressor essentially comprises of a combinational logic circuit with seven inputs and three outputs. It accepts a seven bit input string as input, and produces its sum as output. The conventional architecture of a 7-3 compressor is based on the extended design of a conventional 4-2 compressor. The architecture of a conventional 7-3 compressor is shown in Figure 8. Table II shows the number of different parameters in Tanner EDA used for circuit connections of the 7:3 compressor using different logics.

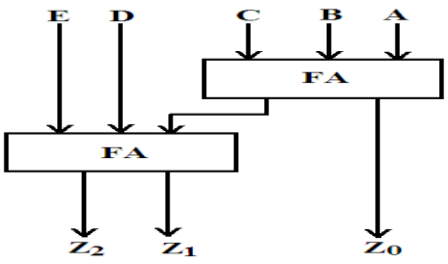


**Figure 7: Architecture of a 5-3 compressor**

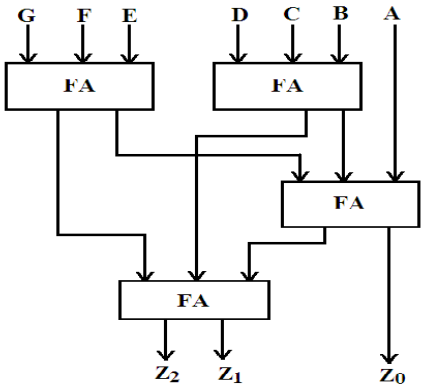


**Figure 8: Architecture of 7-3 compressor**

**TABLE I**
**PARAMETERS USED TO CONSTRUCT THE 5:3 COMPRESSOR USING DIFFERENT LOGIC**

| Parameters | Conv | GDI | TG | ECRL | 14T |
|---|---|---|---|---|---|
| Total nodes | 35 | 17 | 21 | 54 | 17 |
| Active Devices | 56 | 28 | 40 | 80 | 28 |
| Independent Sources | 6 | 6 | 6 | 7 | 6 |
| Passive Devices | 0 | 0 | 0 | 0 | 0 |
| Control Sources | 0 | 0 | 0 | 0 | 0 |
| Total Devices | 62 | 34 | 46 | 87 | 34 |

**TABLE II**
**PARAMETERS USED TO CONSTRUCT THE 7:3 COMPRESSOR USING DIFFERENT LOGIC**

| Parameters | Conv | GDI | TG | ECRL | 14T |
|---|---|---|---|---|---|
| Total nodes | 65 | 29 | 37 | 102 | 29 |
| Active Devices | 112 | 40 | 80 | 160 | 56 |
| Independent Sources | 8 | 8 | 8 | 8 | 8 |
| Passive Devices | 0 | 0 | 0 | 0 | 0 |
| Control Sources | 0 | 0 | 0 | 0 | 0 |
| Total Devices | 120 | 48 | 88 | 168 | 64 |

## IV. SIMULATION RESULTS

Table III shows the average power, delay and PDP for different logic implemented in case of the 5:3 compressor and Figure 9, Figure 10 and Figure 11 respectively shows the variation of average power, delay and PDP for different logic implemented in case of the 5:3 compressor.

**TABLE III**
**AVERAGE POWER, DELAY AND PDP FOR DIFFERENT LOGIC IMPLEMENTED IN CASE OF THE 5:3 COMPRESSORS**

| Logic Style | Average Power in μW | Delay in nS | PDP in W-S |
|---|---|---|---|

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| | | | |
|---|---|---|---|
| Conventional | 29.2 | 1.89 | 5.52E-14 |
| GDI | 3.14 | 0.157 | 4.93E-16 |
| TG | 0.326 | 0.0992 | 3.23E-17 |
| ECRL | 6.16 | 7.12 | 4.39E-14 |
| 14T | 0.334 | 0.0915 | 3.06E-17 |

From Figure 9 it is obvious that the power consumption of all the used logic is better than the conventional logic and from Figure 10 it is obvious that the delay of all the used logic (except ECRL) is better than the conventional logic, but the PDP of all the logic performs better than the conventional one as obtained from Figure 11.

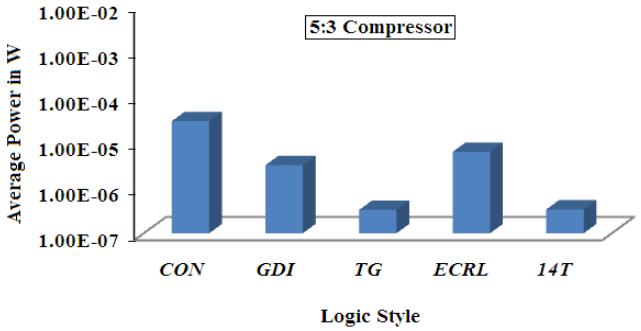


**Figure 9: Average Power comparison of 5:3 compressors**

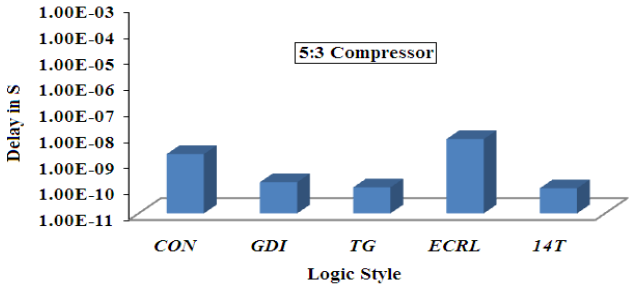


**Figure 10: Delay comparison of 5:3 compressors**

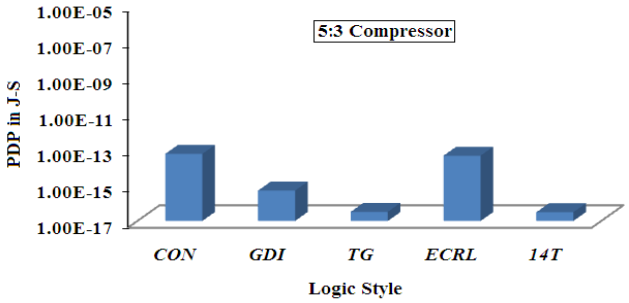


**Figure 11: PDP comparison of 5:3 compressors**

Table IV shows the average power, delay and PDP for different logic implemented in case of the 7:3 compressor and Figure12, Figure 13 and Figure 14 respectively shows the variation of average power, delay and PDP for different logic implemented in case of the 7:3 compressor.

**TABLE IV**
**AVERAGE POWER, DELAY AND PDP FOR DIFFERENT LOGIC IMPLEMENTED IN CASE OF THE 7:3 COMPRESSORS**

| Logic Style | Average Power in μW | Delay in nS | PDP in W-S |
|---|---|---|---|
| Conventional | 47.4 | 1.93 | 9.29E-14 |
| GDI | 22.1 | 1.11 | 2.45E-14 |
| TG | 1.02 | 0.333 | 3.40E-16 |
| ECRL | 25.1 | 7.89 | 1.98E-13 |
| 14T | 0.483 | 0.688 | 3.32E-16 |

From Figure 12 it is obvious that the power consumption of all the used logic is better than the conventional logic and from Figure 13 it is obvious that the delay of all the used logic (except ECRL) is better than the conventional logic.

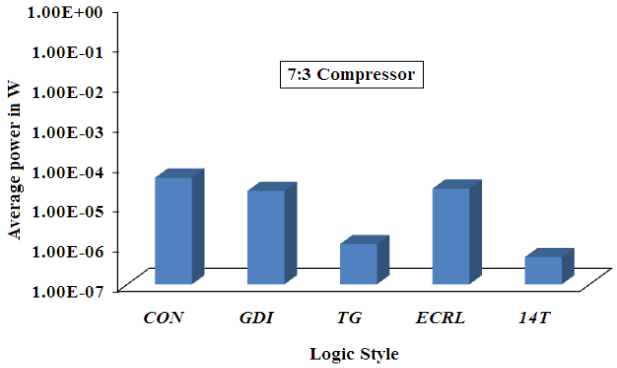


**Figure 12: Average Power comparison of 7:3 compressors**

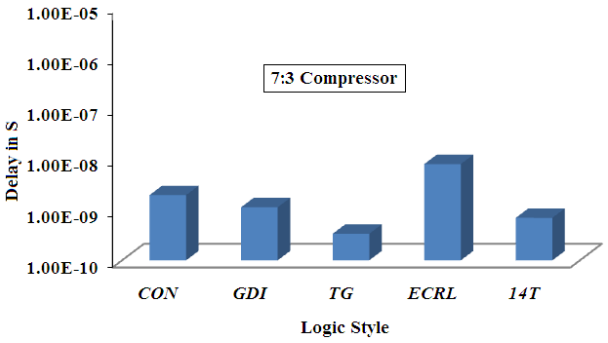


**Figure 13: Delay comparison of 7:3 compressors**

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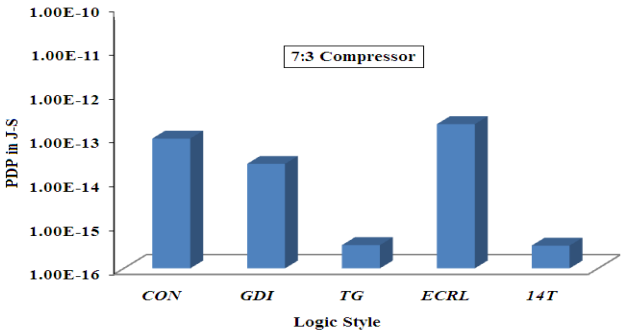


**Figure 14: PDP comparison of 7:3 compressors**

## V. SIMULATION WAVEFORMS

Figure 15 and Figure 16 show the simulated waveforms for a typical set of inputs of the designed conventional compressors. For the input combination, A=01, B=01, C=00, D=00, E=00, the outputs Z0, Z1 and Z2 shows the result in accordance with the graph as shown in Figure 15 for the conventional 5 : 3 compressor.

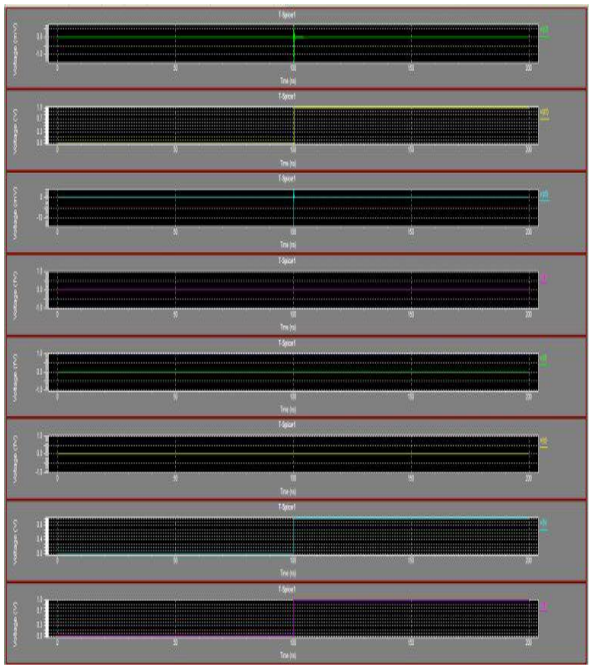

**Figure 15: Simulation waveform of 5:3 compressor in conventional logic**

For the input combination, A=00, B=01, C=00, D=01, E=00, F=01, G=00, the outputs Z0, Z1 and Z2 show the result in accordance with the graph as shown in Figure 16 for the conventional 7 : 3 compressor.

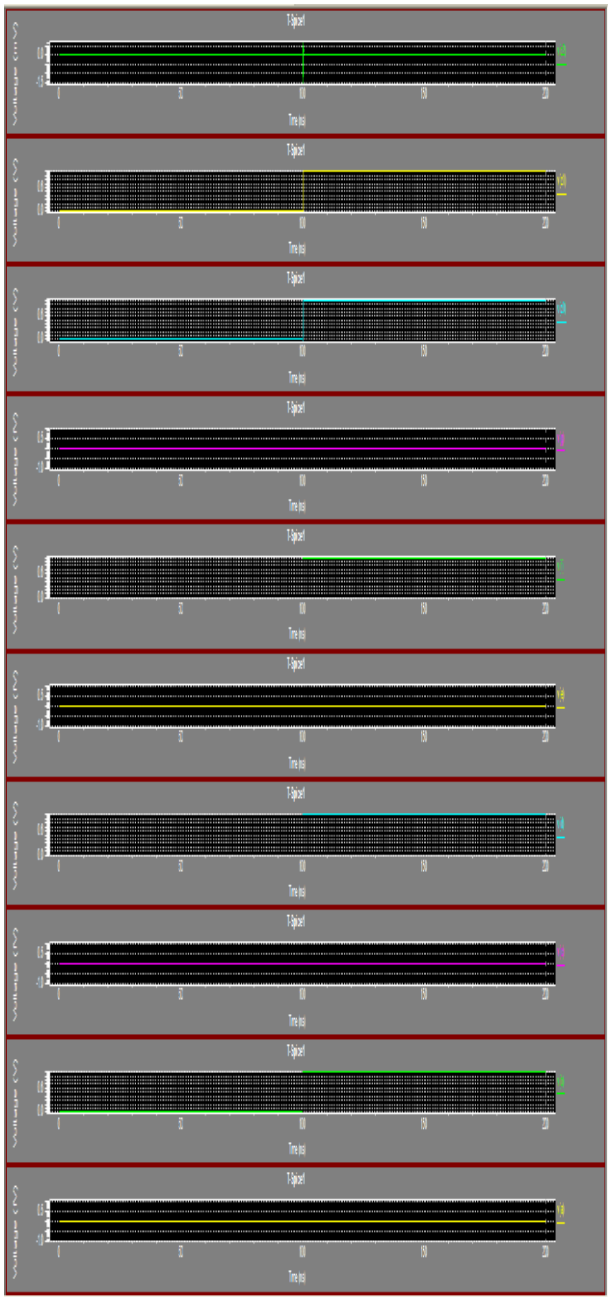

**Figure 16: Simulation waveform of 7:3 compressor in conventional logic**

## VI. CONCLUSION

The use of compressor in DSP is basically to minimize the delay during heavy calculation. It is also considered that for such delay minimization the power consumption can also be as low as possible. So, the aim of every researcher is to minimize the delay with low power consumption to operate the desired compressor at a faster rate. To get the desired performance, the compressors can be tested with efficient adders. Compressor-based multipliers simultaneously reduce the vertical critical path

and the stage operations. 16 bit multiplier effectively utilizes all the above said compressors for partial product reduction. The 14-T and TG full adder based compressors are suitable for partial product reduction in multipliers than the better results of GDI and ECRL. For the requirements of cost efficient computing, the use of diodes in adiabatic logic circuit designs is necessary. Attention must be paid to the current-carrying state of transistors at times when the devices being switched off, as well as the voltage state when the devices are switched on. Though the Adiabatic circuitry consumes more area than the conventional CMOS logic but with respect to consumed energy it gives better performance than the CMOS counterpart.

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