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Manifold Error Recognition and Modification

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ABSTRACT

Hamming codes are attractive as they are simple to construct for any word length and encoding or decoding can be done with low latency. In this paper, modified Hamming codes to enhance adjacent error detection along with double adjacent error correction is presented. The enhanced detection of adjacent errors can be achieved by modifying the Hamming matrices. The double adjacent error correction can be achieved by adding few redundant bits. The modified Hamming codes can correct single and double adjacent errors and can detect double errors and triple adjacent errors. The double and triple adjacent errors are precisely the types of errors that an MCU would likely cause, and therefore, the modified Hamming codes will be useful to provide error detection and correction for MCUs in memory designs.

***Keywords*—**Double Adjacent Error Correction, Error Detection and Correction, Multiple Cell Upset, Single Error Correction

I. INTRODUCTION

Coding theory is concerned with reliability of communication over noise affected channels. Error correcting codes are used in a wide range of communication systems from deep space communication, to quality of sound in compact disks and wireless phones. In the current world, communication has got many applications such as telephonic conversations, deep space communication, remote monitoring, digital video broad casting, navigation etc. in which the messages are encoded into the communication channel and then decoding it at the receiver end. Digital communications and storage have become part of our daily lives. During the transfer of message, the data might get corrupted due to occurrence of lots of disturbances in the communication channel. Errors in data transmission or storage systems can come from many different sources: random noise, interference, channel fading, or physical defects, just to name a few. These channel errors must be reduced to an acceptable level to ensure the quality of data transmission or storage. Nowadays multiple errors are becoming more frequent as integration scale increases. Multiple errors occur mainly to adjacent bits. So it is necessary for the decoder tools to have a function of correcting the error that might occur.Digital data is transmitted over a channel and there will be noise in the channel.The noise may distort the messages to be sent. Thus, what the receiver receives may not be the same as what the sender sends. The goal of coding theory is to improve the reliability of digital communication by devising methods that enable the receiver to decide whether there have been errors during the transmission (error detection), and if there are, to possibly recover the original message (error correction). Error Correction Codes (ECCs) are used to prevent soft errors from causing datacorruption in memories and registers. The codes used range from simple codes such asHamming codes to more powerful and complex codes like Bose Chaudhuri Hocquenghem(BCH) codes, matrix codes and Euclidean Geometry (EG) codes. In all cases, the datais encoded when it is written into the memory and decoded when it is read. One exampleof codes for which decoding can be done with low delay is Single Error Correction (SEC)codes. Hamming codes are Single error correction codes. Hamming codes are attractiveas they are simple to construct for any word length and the encoding-decoding can bedone with low delay. SEC codes have a minimum distance of three and therefore adouble error can be mistaken for a single error and erroneously corrected. To avoid this issue Single Error Correction Double Error Detection (SEC-DED) codes are preferredin memory applications; these codes have a minimum distance of four.

II. PRIOR APPROACH

Error detection and correction are techniques that enable reliable delivery of digital data over unreliable communication channel. Many communication channels are subject to channel noise, and thus errors may be

introduced during transmission from the source to a receiver. The overallclassification of error detection and correction schemes is shown in Figure 2.1.
Different error correcting codes can be used depending on the properties of the system and the application in which the error correcting is to be introduced. Basically, error detecting and correcting codes have been classified into block codes and convolution codes. The main difference between these two codes is the presence or absence of memory in the encoder.

In the block code, the incoming data bit is divided into blocks andeach block is processed individually by adding redundancy or parity bits accordance with a prescribed algorithm[2]. The decoder processes each block individually and corrects errors byseparating redundancy.Accordingly, the encoder for a convolution code operates on the incoming message sequence,using a sliding window equal in duration to its own memory. Hence in a convolutioncode, unlike a block code where code words are produced on a block by block basis,the channel encoder accepts message bits as continuous sequence and thereby generatesa continuous sequence of encoded bits at a higher rate.

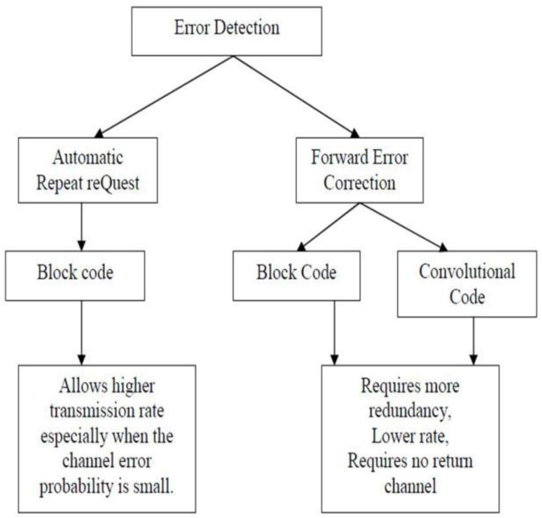

Error Detection
Automatic Repeat reQuest
Forward Error Correction
Block code
Block Code
Convolutional Code
Allows higher transmission rate especially when the channel error probability is small.
Requires more redundancy, Lower rate, Requires no return channel

Fig.2.1Error detection and correction schemes

An error-correcting code (ECC) is a system of adding parity bits, to a message, such that it can be recovered by a receiver even when a number of errors were introduced, either during the process of transmission, or on storage. Since the receiver does not have to ask the sender for retransmission of the data, a backchannel is not required in forward error correction, and it is therefore suitable for simplexcommunication such as broadcasting. Error correcting codes are also frequently used for reliable storage in media such as CDs, DVDs, hard disks, and RAM.

2.1 Error Detection Scheme

Someof the Error detection schemesare discussed below:
Parity scheme: In parity scheme, all the data sets are assigned a particular parity i.e. either even or odd. In the receiver parity of received data is checked. Receiver check whether it satisfy the assigned parity. If not, it is found to be in error. It is effective only for odd number of errors.***Checksum Scheme*:** In this scheme, a checksum is calculated in the transmitter and sent with the actual data. In receiver checksum is calculated and compared with the received checksum. A mismatch is an indication of error.
***Cyclic Redundancy Check scheme*:** In this scheme, the message is interpreted as polynomial and is divided by a generator polynomial. Then the reminder of the division is added to the actual message polynomial to form a code polynomial. The generator polynomial is divided to this code polynomial. This property is checked by the receiver. If failed to satisfy this property the received code word is in error. It is complex but efficient error detection scheme.
***Hamming distance Based Check scheme*:** This scheme is basically parity based scheme but here parity of different combination of bits are checked for parity. It can detect double errors and can correct single errors.
***Polarity scheme*:** In this scheme, the actual message along with its inversion format. Inreceiver, it is checked whether two sets are inverse of each other. If not it is an indication of error. It will not be able to detect the error if the corresponding bits in the data and its inverse are in the error.

2.2 Error Correction

Automatic repeat request (ARQ):

Retransmission of the data is requested if the check fails when each blocks of the data received is checked using error detection code. This may be done repeatedly, until the data can be verified.Transmitter retransmits the frame until it receives the acknowledgement within a reasonable amount of time after sending the data frame. Stop-and-waitARQ, Go-Back-N ARQ, and Selective Repeat ARQ are the three types of ARQ protocols. ARQ is suitable for the communication channel having varying capacity or if its capacity is unknown like in the case of Internet.The drawback of ARQ is latency due to retransmissions, and requires the maintenance of buffers and timers forretransmissions.

Forward error correction (FEC):

The sender encodes the data using an error correctingcode (ECC) prior to transmission. The additional information (redundancy) added bythe code is used by the receiver to recover the original data. In general, the reconstructeddata is what is deemed the "most likely" original data. There are several ways ofclassifying the forward error correction codes as per different characteristics.

Linear vs. Nonlinear: Linear codes are the sum of any two valid codewords is also a valid code word. In case of nonlinear code the above statement is notalways true.

***Cyclic vs. Non-Cyclic*:** Cyclic code word is those in which shifting of any valid codeword is also a valid code word. In case of non circular code word the above statementis not always true.

***Systematic vs. Nonsystematic*:**Actual message remain unaltered in the code and redundant bit added to the message to detect and correct errors. In nonsystematic code the actual message does not appear in itsoriginal form in the code rather there exists one mapping method from the data word to code word and vice versa.

***Block vs. convolution*:** The block codes are those in which one block of messageis transformed into on block of code. In this case no memory is required. In case ofconvolution code a sequence of message is converted into a sequence of code whereencoder requires memory as present code which is a combination of present and past message.

***Binary vs. Non binary*:** Binary codes are those in which error detection and correction is done on binary information i.e. on bits. After detecting the position of error, correction done only by flipping that erroneous bit. In Non binary code, the entire process is done on symbols.

III. PROPOSED CODE

The code was proposed in Hsiao and Hamming code for single error correction and double adjacent error detection and correction. Hsiao code derives an optimal minimum parity checking relationship, which reduces implementation logic depth and gate count. Both Hsiao and Hamming codes provide single bit correction and double bit detection and correction capabilities. Both codes require the same number of check bits for a specific data word length.

The parity check matrix for the Hsiao code is constructed as follows:

1. Assuming r check bits (c_{r-1}, c_{r-2}. . . c_1, c_0), an r-bit column with a single 1 is assigned to check bit c_i; the bit position i (from top) in that column is 1; all other bit positions are 0.

2. If the length of the information bits is k and ${}^{r}C_3$ (combinations of c_{r-1}, c_{r-2}. . . c_1, c_0 which have three 1s) > k, k columns out of ${}^{r}C_3$ combinations are selected such that each of these columns has three 1s. If ${}^{r}C_3 < k$, all ${}^{r}C_3$ columns are selected; the remaining columns are selected first from among ${}^{r}C_5$ columns having five 1s, then fromamong ${}^{r}C_7$ columns having seven 1s, and so on. This process is continued until all kcolumns in the parity check matrix have been specified.

The Hsiao code for k = 8 is illustrated below as an example. The number of checkbits required to correct single bit and detect double bit inversions is r = 5. Each check bit is assigned a 5 bit column as shown in figure 3.1.

$$\begin{array}{ccccc}
c_4 & c_3 & c_2 & c_1 & c_0 \\
0 & 0 & 0 & 0 & 1 \\
0 & 0 & 0 & 1 & 0 \\
0 & 0 & 1 & 0 & 0 \\
0 & 1 & 0 & 0 & 0 \\
1 & 0 & 0 & 0 & 0
\end{array}$$

Fig.3.1 Check bit is assigned a 5 bit column

since ${}^{r}C_3={}^{5}C_3=10$ is greater than k = 8, any eight columns out of 10 having three 1s can be assigned to the information bits.

Assuming d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0 are the information bits, a column assignment is selected for these bits, which, together with previously assigned check bits, forms the parity check matrix for the (12, 8) Hsiao code, as shown in figure 3.2.

$$\left|\begin{array}{ccccccccccccc}
d_7 & d_6 & d_5 & d_4 & d_3 & d_2 & d_1 & d_0 & c_4 & c_3 & c_2 & c_1 & c_0 \\
0 & 1 & 1 & 0 & 1 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 1 \\
1 & 0 & 1 & 1 & 0 & 1 & 1 & 0 & 0 & 0 & 0 & 1 & 0 \\
1 & 1 & 1 & 0 & 0 & 0 & 1 & 1 & 0 & 0 & 1 & 0 & 0 \\
1 & 0 & 0 & 1 & 1 & 0 & 0 & 1 & 0 & 1 & 0 & 0 & 0 \\
0 & 1 & 0 & 1 & 1 & 1 & 1 & 1 & 1 & 0 & 0 & 0 & 0
\end{array}\right|
\begin{array}{c} \\ e_0 \\ e_1 \\ e_2 \\ e_3 \\ e_4 \end{array}$$

Fig.3.2 Parity check matrix for the (12, 8) Hsiao code

From the matrix the check bit equations are derived as follows:

$c_0=d_6$ xor d_5 xor d_3 xor d_2

$c_1=d_7$ xor d_5 xor d_4 xor d_2 xor d_1

$c_2=d_7$ xor d_6 xor d_5 xor d_1 xor d_0

$c_3=d_7$ xor d_4 xor d_3 xor d_0

$c_4=d_6$ xor d_4 xor d_3 xor d_2 xor d_1 xor d_0

For example, if

d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0 =00110011 then the parity check bits are

c_4 c_3 c_2 c_1 c_0 =10111

Now, let us assume bit d_4 has changed from 1 to 0. The check bits can be recomputedas:

$c_4^T c_3^T$ c_2^T c_1^T c_0^T= 01101

Therefore the syndrome bits are:

$e_0=c_0$ xor $c_0^T=0$

$e_1=c_1$ xor $c_1^T=1$

$e_2=c_2$ xor $c_2^T=0$

$e_3=c_3$ xor $c_3^T=1$

$e_4=c_4$ xor $c_4^T=1$

It can be seen that the syndrome bits match with the fourth column from the left in the parity matrix, identifying d_4 as an erroneous bit.

Next, we can consider a double-bit inversion. For example, d_1 d_0 changed from 11 to 00.
Then the recomputed check bits are:
$c_4^T c_3^T c_2^T c_1^T c_0^T$=11101
The resulting syndrome bits are:
e_4 e_3 e_2 e_1 e_0=01010

Since this does not match with any column of the parity check matrix and the overallparity of the syndrome bits is 0, a double bit error is present. Note that the syndromevector matches with the EX-OR of columns d_1 d_0 in the parity check matrix (d1d0 arethe bits where bit-inversions were inserted).

The modified Hamming code (12, 8) consist of parity check matrix called lexicographic matrix is shown below in Figure 3.6

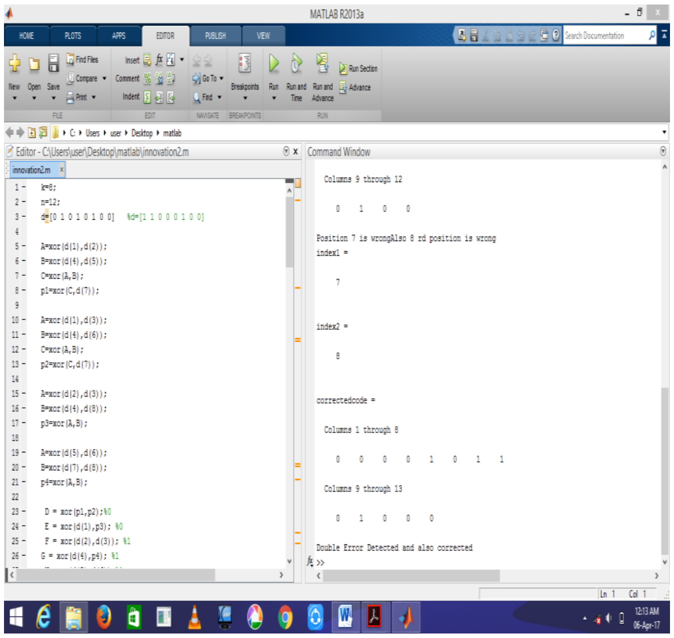
$$H_{Lex}=\begin{pmatrix} 0&0&0&0&0&0&0&1&1&1&1&1\\ 0&0&0&1&1&1&1&0&0&0&0&1\\ 0&1&1&0&0&1&1&0&0&1&1&0\\ 1&0&1&0&1&0&1&0&1&0&1&0 \end{pmatrix}$$

Fig.3.3Lexicographic check matrix.

If a single bit error occurs in the code word, the syndrome vector is the product of the lexicographic matrix with the error code word gives the binary representation of the position where the error was inserted. Using as an example Hammingcode (12, 8), data bits (01010100) are coded as (000010110100). When an error occursand, for instance, the third bit is changed the code word turns into (001010110100). Theproduct of this vector by the lexicographic check matrix results in the syndrome vector(1100) corresponding to the binary representation of three. In this case, the extended Hamming code (13, 8) encodes (01010100) into (0000101101000).If we include this additionalparity bit, the previous 12-bit coded word becomes 001110010100P13, where P13 isevaluated from the exclusive-OR of the other 12 bits. This produces the 13-bit word0011100101001 (even parity). When this codeword is read from the memory, the check bits and also the parity bit P are evaluated over the entire 13 bits. If P = 0, the parity is correct(even parity), but if P = 1, the parity over the 13 bits is incorrect (odd parity).

IV. SIMULATION RESULTS

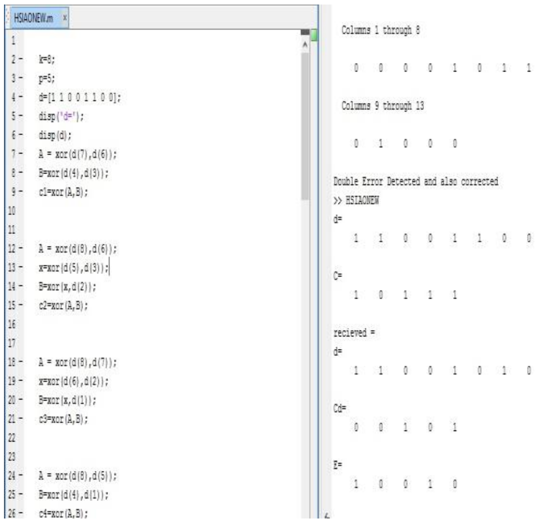
The code for the proposed Hsiao and Hamming code for single error correction and double adjacent error detection and correction was written in MATLAB and the code was simulated on MATLAB R2013a. It was tested for correct functionality by giving various inputs.



```
k=8;
n=12;
d=[0 1 0 1 0 1 0 0]    %d=[1 1 0 0 0 1 0 0]

A=xor(d(1),d(2));
B=xor(d(4),d(5));
C=xor(A,B);
p1=xor(C,d(7));

A=xor(d(1),d(3));
B=xor(d(4),d(6));
C=xor(A,B);
p2=xor(C,d(7));

A=xor(d(2),d(3));
B=xor(d(4),d(8));
p3=xor(A,B);

A=xor(d(5),d(6));
B=xor(d(7),d(8));
p4=xor(A,B);

 D = xor(p1,p2);%0
 E = xor(d(1),p3); %0
 F = xor(d(2),d(3)); %1
G = xor(d(4),p4); %1
```

```
  Columns 9 through 12

     0     1     0     0

Position 7 is wrongAlso 8 rd position is wrong
index1 =

     7


index2 =

     8


correctedcode =

  Columns 1 through 8

     0     0     0     0     1     0     1     1

  Columns 9 through 13

     0     1     0     0     0

Double Error Detected and also corrected
>>
```

Fig.4.1Simulation result of Hamming code



```

k=8;
p=5;
d=[1 1 0 0 1 1 0 0];
disp('d=');
disp(d);
A = xor(d(7),d(6));
B=xor(d(4),d(3));
c1=xor(A,B);


A = xor(d(8),d(6));
x=xor(d(5),d(3));
B=xor(x,d(2));
c2=xor(A,B);


A = xor(d(8),d(7));
x=xor(d(6),d(2));
B=xor(x,d(1));
c3=xor(A,B);


A = xor(d(8),d(5));
B=xor(d(4),d(1));
c4=xor(A,B);
```

```
  Columns 1 through 8

     0     0     0     0     1     0     1     1

  Columns 9 through 13

     0     1     0     0     0

Double Error Detected and also corrected
>> HSIAONEW
d=
     1     1     0     0     1     1     0     0

C=
     1     0     1     1     1

recieved =
d=
     1     1     0     0     1     0     1     0

Cd=
     0     0     1     0     1

E=
     1     0     0     1     0
```

Fig.4.2 Simulation result of Hsiao code

V. CONCLUSION

A modified Hamming code that can generate and check parity bits for a single error correction, adjacent double-error-detection and correction scheme is most often used in real systems. Hamming codes are attractive as they are simple to construct for any word length and the encodingand decoding can be done with low delay. The complex codes like BCH, RS codes require large registers in the encoding and decoding section. Thus, this paper proposed the code which mostly effective in applications like aircrafts where light weight registers having encoder & decoder having error detection and correction codes.

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