Modelling of Hybrid CMOS-SET based Highly Efficient Parallel-In-Serial-Out Shift Register for Next Generation Electronics

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ABSTRACT

Single electronics, a comparatively new field of solid state science and technology, has been developed speedily in both theory and experiments because the essential e-beam lithography techniques have matured enough during the past two decades. Research in this field ushered promising domino effect for near future. In spite of numerous advantages, the fragility in fully exploring the properties of Single Electronic Transistors (SET) and further manipulating them in new architectures by which they can be integrated on a single chip remains a challenge. But thereafter, un-put-down-able device scientists then articulated hybridization of existing CMOS technology with SETs to overcome the specific drawbacks of SET and to explore new horizon in device research. Here a similar attempt to realize hybrid CMOS-SET based Parallel-In-Serial-Out Shift Register is revealed to investigate the robustness and fastness of the novel architecture by comparing it with existing CMOS technology. The consequences besides being impressive bears better validation to incorporate the model in near future.

Keywords—Single Electronic Transistor, Hybrid CMOS-SET, Parallel-In-Serial-Out Shift Register, Lithography

I. INTRODUCTION

Giga-scale ICs inherently requires fewer electrons in device action so that power consumption and battery voltage reduce considerably. This is quite complex to achieve in conventional devices due to statistical fluctuations in electron numbers resulting noise. Thus an innovative technology was invented namely SET technology which employs the possibility and controls the movement and position of a single electron or a small number of electrons. The fundamental principle of single electronics is the Coulomb blockade, first observed and considered by Gorter [1] in an empirical study. SETs employ the Coulomb blockade (CB), which occurs in tiny die area made from conductive material due to the electrostatic interactions of confined electrons. The processes of Coulomb blockade, single-electron tunneling and related phenomena from the physical point of view have been categorically demonstrated in semiconductor single-electron transistors, metallic nanostructure devices, low-dimensional organic nanostructures, and III–V compound semiconductors etc [2, 3]. More conveniently, in IC structures, single-electron tunneling takes place through the resonant tunneling process between discrete energy states in one or more of the junction nodes.

In SET made devices, one bit of information is represented by a few numbers of electrons. Extremely low operational power gets to the bottom of some of the instability and reliability problems. Owing to such intrinsic potentials Single electron devices (SED) so far proposed in the literature include single electron transistors (SETs) [4, 5], single electron memories [6,7], dot-based cellular automata [8, 9], binary decision devices [10], inverters [11], pumps [12], majority gates [13], analog to digital converter [14], logic gates [15], single electron latches and buffers [16] and several circuits [17] etc.

Amid all distinctive merits, SET posses some drawbacks of poor current driving capabilities and lack of room temperature operable technology. Until one triumph over the fragilities of SETs, in near future, complete replacement of MOSFET by SET is not possible. Alternatively, CMOS is rewarded with the blessings of high voltage gain, high driving speed and also high input impedance. Thus there lays a profound prospect to adapt hybrid CMOS-SET so that it can compensate the intrinsic drawbacks of SET. Thus the unconventional solution to assemble the circuit in hybrid structure by a combination of SET and conventional devices like CMOS for VLSI and ULSI circuits [18] is gaining recognition.

In section II we refer to the SET theory including its advantages and disadvantages. It is followed by a comparative study of CMOS and SET in section III. Next a hybrid CMOS-SET model for the Parallel-In-Serial-Out Shift Register is proposed in section IV. Lastly, section V presents the justification of the novel hybrid architecture.
II. THE CONCEPT OF SET

As seen from the constructional point of view, Single electron transistor is similar to an Electron Island that has two separate junctions for electron entrance and exit of a single electron with two gates attached to it. Basically one gate tunes the voltage of the whole structure whereas the other one controls the number of electrons coming in and out of the island one at a time. The conduction process is driven by Coulomb-Blockade principle. The device initiates by overcoming the critical voltage $V_c$ of a tunnel junction: $V_c=q/[2(C_e+C_j)]$, where, $C_j$ is the capacitance of tunnel junction & $C_e$ is the equivalent capacitance beheld from the junctions perspective and $q$ is the electronic charge. The flow of an electron through a tunnel junction being a stochastic process takes time and is defined as switching delay $T_d$.

Fig. 1 depicts a single-electron transistor which consisting of two tunnel junctions placed in series known as a Coulomb island where electrons can tunnel through one of the insulators. The three terminals of the device are: the outside lead of each tunnel junction and a gate terminal which is capacitively coupled to the node between the two tunnel junctions. The capacitor provides the setting of electric charge on the Coulomb Island. No tunneling or very little tunneling is possible through the two tunnel junctions when the gate voltage is set to zero. The tunneling current considerably increases with the gate voltage raised to $e/2C$.

In Fig. 2 the tunneling operations of electrons are elucidated. The process is that if an electron approach towards ‘Q’ and pulse $\Phi_{m1}$>5mV is applied, then the electron can tunnel through the junctions (J1 or J3) to ‘S’ or ‘U’ depending on whether the sum of Coulomb energy $[E_c=e^2/(2C_j)]$ + applied energy is greater than the potential height of the barrier energy of junction(s) J1 or J3. This principle let the electron follow the path ‘QRST’ or ‘QRUV’ on condition that the signal $X_i$ > 5mv and the corresponding total energy is greater than the static potential junction energy of J2 or J4 [19-21].

Keeping in view the circuit design considerations of SET based devices - it proceeds in two different architectures. One being the hybrid CMOS-SET architecture which provides high voltage gain & driving ability and removes low power feature of SETs partially, the other is the SET’s only architecture where the charge transport through the junction is essentially considered to be of one electron. In the present work the first architecture is selected to proceed because of the findings of section III.

III. A CHRONICLE STUDY OF SET AND CMOS

SET provided innumerable rewards including – (i) The electron conduction in SET is performed in one by one step, whereas many electrons simultaneously participate in conduction of CMOS. (ii) It offers a greater scaling potential than CMOS because the device structure is quite simple. (iii) SET posses higher potential to realize circuits that can operate without consuming high energy than any other existing CMOS circuits. (iv) A recent advancement in silicon based fabrication technology enlightens the possibilities to realize SET circuits to operate at room temperature and (v) Further, the tunnel junctions that are known to be the basic circuit element of SET have the potential to be fabricated in simplistic ways [22].

But, SETs posses high output impedance and are sensitive to random background charges. This makes it unlikely that SETs would ever replace CMOS-FETs in applications where large voltage gain or low output impedance is necessary [23, 24]. Other prominent factors preventing the use of SETs in most applications are the (i) low gain, (ii) the high output impedance and (iii) the background charges and (iv) room temperature operations.

As SETs are made smaller, there is an increase in operating temperatures, in operating frequency as well as in device packing density. However, some of the circuit architectures that have been proposed for single-electron transistors are basically copies of the semiconducting architectures which require SETs with voltage gain. Because of this limitation of SETs, it now seems that it has to go under extensive research before commercially designing a SET based dense integrated circuits using the existing technology. To the contrary, a transistor does not necessarily have to exhibit voltage gain to be considered as useful. However, for SETs, it is more important to consider the charge gain; this can be easily achieved only beyond room temperature. Charge gain would be used in situations where charge needs to be measured, for instance to readout a memory cell or to readout a charge coupled device. The speed of the charge readout would be limited by the RC-delay formed by the resistance of the SET and the capacitance at the output of the SET. The large output impedance of a SET of at least 100K makes the SET an intrinsically slow device [25, 26]. The background charge problem is another important issue that is inhibiting the widespread use of SETs [27-30]. The origin of the background charge problem is the extreme charge sensitivity of SETs. A single charged vacancy or an interstitial ion in the oxide near a SET can be enough to switch the transistor from being conducting to being non-conducting. The same kinds of charged defects are present and move in FETs but most FETs are not as sensitive to charge so the consequences of those background charges are not as great.

Now considering the merits of existing and highly proficient as well as much matured CMOS technology are – (i) High gain and current drive, (ii) High speed, (iii) Very matured e-beam lithography based fabrication technology and (iv) Huge research studies with empirical results are available; whereas sub-10-nm physical limits and Power density are some of the intrinsic limitations of it.

Therefore, ample study focused that a complete replacement of CMOS by SET is quite time consuming
and it is not in proximity in very near future; it is also true that by combining SET and CMOS, i.e., hybridizing CMOS-SET can bring out new functionalities, which are not represented in pure CMOS technology. Such a co-integration approach also glides the sudden transformation of technology from CMOS to SET [31, 32]. Thus the concept of hybrid CMOS-SET architectures has already captivated higher attention both in industry and academics. Toshiba successfully demonstrated the performance of a hybrid MOS-SET inverter on a SOI wafer [33, 34] with improved gain at transition levels but the current drive remains low. This is why the authors here adhered to hybrid CMOS-SET co-integration to design the Parallel-In-Serial-Out Shift Register.

IV. MODELLING OF HYBRID CMOS-SET BASED PARALLEL-IN-SERIAL-OUT SHIFT REGISTER

Researchers at Delft University in Netherlands recommended a SPICE simulation package for SET circuit [35] using the Orthodox theory of SET. The authors here follow the SET-MOS quaternary transmission gate [36] which is highly accredited and mostly cited in reputed journals. The co-integration model of Parallel-In-Serial-Out Shift Register were designed and further simulated on this above cited SPICE soft-computing layout which allows place sharing of SETs with the conventional MOS devices in one particular die area as elucidated in Fig. 3. More conveniently, the logic operations of the proposed circuit were first tested by simulation using T-Spice simulation software. Thereafter, MIB compact model for SET device and BSIM4.6.1 model for CMOS was incorporated for obtaining detailed empirical results which are briefly included in this presentation.

The modus operandi of the hybrid CMOS-SET Parallel-In-Serial-Out Shift Register is analytically studied here in this section. To achieve maximum rendering of the SET structure i.e., to make it function as a switch, the SET is pushed up into the Coulomb blockade state which denotes an ‘OFF’ condition or else it can be permitted to conduct current i.e., the ‘ON’ condition; subsequently it posses mimic MOSFET logic architecture and develops perfect co-residing with CMOS and develops all potentials to obtain better trade off in a hybrid CMOS-SET logic family. The structural co-integration is formed by locating a PMOS transistor as the load resistance of an SET. The uniqueness lies here in this technology is that the PMOS transistor has the SET at its load in the gates. We considered some design rules and they were implied before practical hybrid CMOS-SET circuit design using SPICE. Considering the overview of the novel Parallel-In-Serial-Out Shift Register structures, it resembles CMOS inverter; but there are two basic differences, i.e., (i) the ‘Pull Up’ transistor is an SET and (ii) the $V_{DD}$ is defined by the SET device parameters.

V. COMPARATIVE STUDY OF THE PROPOSED MODEL

The present work explored the highest implementation of hybrid CMOS-SET logic gates in one of the most complex circuit; undoubtedly the presented model of Parallel-In-Serial-Out Shift Register can be included in BIOS architecture for next generation electronics. The proposed model showed no errors in performing the logic operations, rather two distinctive drawbacks of SET circuit was neutralized. Moreover, the power consumptions & propagation delays when compared to CMOS technology were found quite less in hybrid CMOS-SET technology. Table-I below indicates the estimated values of power consumption of the logic gates employed in these two circuits. The output voltage gain is approximated about 4.8 as obtained from the slope of the transitional region. Employing a uniform interval clock pulse the model delivers uninterrupted potentiality and is efficient enough to conduct a predetermined sequence of states. The present projected conception of hybrid CMOS-SET Parallel-In-Serial-Out Shift Register architecture shows satisfaction in trade-off between CMOS and SET.

### Table I

<table>
<thead>
<tr>
<th>Circuit type</th>
<th>Power Supply</th>
<th>No. of CMOS</th>
<th>No. of SET</th>
<th>Power Consumption</th>
</tr>
</thead>
<tbody>
<tr>
<td>AND Gate</td>
<td>0.01V</td>
<td>3</td>
<td>3</td>
<td>1.02E-09 W</td>
</tr>
<tr>
<td>OR Gate</td>
<td>0.01V</td>
<td>3</td>
<td>3</td>
<td>1.02E-09 W</td>
</tr>
<tr>
<td>D Flip-flop</td>
<td>0.01V</td>
<td>9</td>
<td>9</td>
<td>4.12E-09 W</td>
</tr>
</tbody>
</table>

VI. CONCLUSION

The design and simulation of hybrid CMOS-SET Parallel-In-Serial-Out Shift Register is modeled successfully and the results are obtained categorically to expose the underlying potential of perfect co-integration of CMOS-SET. One remarkable attribute is that the SET and CMOS are placed in series and thereby the hybridization achieved improves the gain of the models and simultaneously the propagation delay is lessened to some extent. Based on the hybrid CMOS-SET logic gates, the model was designed and implemented using sophisticated simulation software. The T-Spice simulation results of the proposed model are not only satisfactory but also the feasibility of using the proposed hybrid circuit in future low power ultra-dense VLSI/ULSI electronics is justified. Furthermore, co-integration using hybrid CMOS-SET has a specific advantage that the room temperature operational limitations of SETs are controlled and further the model can exhibit its full functionalities. Beside other remarkable consequences, when the operating temperature lays near to sub ambient regime the switching speed, mobility and
power dissipation shows enhanced performance. Thus the authors here anticipate that the novel hybrid CMOS-SET architecture of Parallel-In-Serial-Out Shift Register will be incorporated in next generation electronics.

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LIST OF FIGURES

Figure 1: SET consisting of two tunnel junctions

Figure 2: SET's basic operation of tunnel junction

Figure 3: Hybrid CMOS-SET based Parallel-In-Serial-Out Shift Register