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Power Optimization by Using Multi-Bit Flip-Flops

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ABSTRACT

A significant portion of the total power consumption in high performance digital circuits in deep submicron region is mainly due to leakage power. Leakage is the only source of power consumption in an idle circuit. Therefore it is important to reduce leakage power in portable systems. Clock gating is a predominant technique used for power saving. It is observed that the commonly used synthesis based gating still leaves a large amount of redundant clock pulses. Data-driven gating aims to disable these. To reduce the hardware overhead involved, flip-flops (FFs) are grouped so that they share a common clock enabling signal.

***Keywords*—**Flip-Flop, Latch, Multibit Flip-Flop, Power Reduction, VLSI.

I. INTRODUCTION

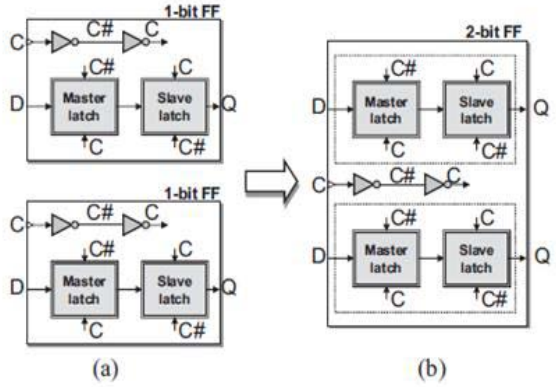
Tools require the employment of a long chain of automatic synthesis algorithms, from register transfer level (RTL) down to gate level and net list. Unfortunately, such automation leads to a large number of unnecessary clock togglings, thus increasing the number of wasted clock pulses at flip-flops (FFs) Consequently, development of automatic and effective methods to reduce this inefficiency is desirable. In the sequel, we will use the terms toggling, switching, and activity interchangeably.

The Clock gating is a predominant technique used for power saving. It is observed that the commonly used synthesis-based gating still leaves a large amount of redundant clock pulses.[1]

The Dynamic power management (DPM) is a design methodology for dynamically reconfiguring systems to provide the requested services and performance levels with a minimum number of active components or a minimum load on such components[2].

Reducing the power consumption of a synchronous digital system by minimizing the total power consumed by the clock signals. We construct activity-driven clock trees wherein sections of the clock tree are turned off by gating the clock signals[3]. A method to reduce the power consumption of the popular linear feedback shift register. The proposed scheme is based on the gated clock design approach and it can offer a significant power reduction, depending on technological characteristics of the employed gates[4].

II. BLOCK DIAGRAM



a. Two 1 one bit flip-flops before merging
b. Flip-flops after merging

The nature of this thesis is to implement a software based frequency synthesizer and evaluate the effectiveness, thus the research questions that this particular paper will answer are the following:

Why sequential circuits using cmos for leakage power reduction?

To develop and examine the different designs to make it understandable for designer. The rapid growth in semiconductor device industry has led to the development of high Performance potable systems with enhanced reliability. In such portable applications, it is extremely important to minimize current consumption due to the limited availability of battery Power.

Consequently, power dissipation is becoming recognized as a top priority issue for VLSI circuit design. Clock gating is a predominant technique used for power saving. It is observed that the commonly used synthesis based gating still leaves a large amount of redundant clock pulses. Data-driven gating aims to disable these. To reduce the hardware overhead involved, flip-flops (FFs) are grouped so that they share a common clock enabling signal. Here we answer the question of which FFs should be placed in a group to maximize the power reduction.

A FF finds out that its clock can be disabled in the next cycle by XORing its output with the present data input that will appear at its output in the next cycle. The outputs of *k* XOR gates are ORed to generate a joint gating signal for *k* FFs, which is then latched to avoid glitches. The combination of a latch with AND gate is commonly used by commercial tools. Such data driven gating is used for a digital filter in an ultralow-power design.

In our thesis instead of grouped flip flop we are using D flip flop. By using this memory element we can implement a low power and high speed design. In this proposed system the leakage current flowing through a stack of series connected transistors reduces when more than one transistor of the stack is turned OFF to produce "Stacking Effect". When two or more transistors that are switched OFF are stacked on top of each other then they dissipate less leakage power than a single transistor that is turned OFF. This is because each transistor in the stack induces a slight reverse bias between the gate and source of the transistor right below it, and this increases the threshold voltage of the bottom transistor making it more resistant to leakage.

III. DESIGINING OF MULTIBIT FLIPFLOPS

In electronics, a flip-flop or latch is a circuit that has two stable states and can be used to store state information. A flip-flop is a bistable multivibrator. The circuit can be made to change state by signals applied to one or more control inputs and will have one or two outputs. It is the basic storage element in sequential logic. Flip-flops and latches are a fundamental building block of digital electronics systems used in computers, communications, and many other types of systems.

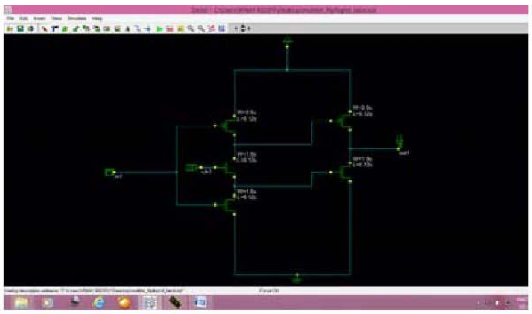


Figure 1: Flip Flop schematic

Flip-flops and latches are used as data storage elements. Such data storage can be used for storage of *state*, and such a circuit is described as sequential logic. When used in a finite-state machine, the output and next state depend not only on its current input, but also on its current state (and hence, previous inputs). It can also be used for counting of pulses, and for synchronizing variably-timed input signals to some reference timing signal.

Flip-flops can be either simple (transparent or opaque) or clocked (synchronous or edge-triggered); the simple ones are commonly called latches. The word latch is mainly used for storage elements, while clocked devices are described as flip-flops.

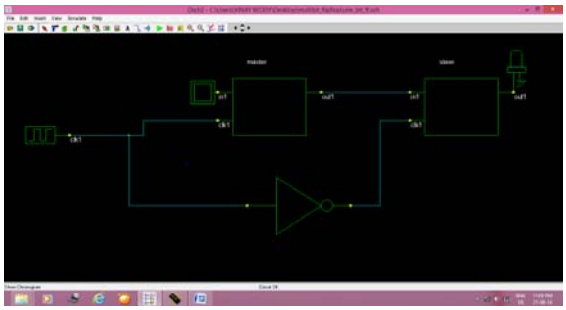


Figure 2: Latch schematic

A latch is level-sensitive, whereas a flip-flop is edge-sensitive. That is, when a latch is enabled it becomes transparent, while a flip flop's output only changes on a single type (positive going or negative going) of clock edge.

The electronic devices we encounter all around us are driven and controlled by the flow of electrical current through electronic circuits. Each circuit is an arrangement of electrical elements designed to perform specific functions. Circuits can be engineered to carry out a wide variety of operations, from simple actions to complex tasks, according to the job(s) the system must perform.

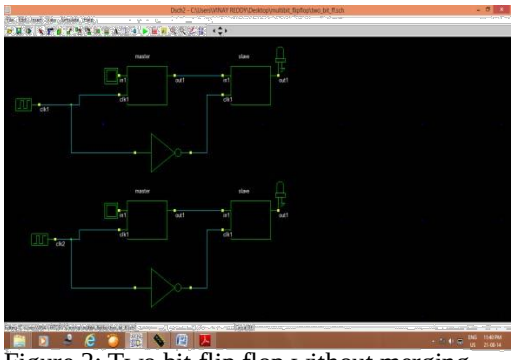


Figure 3: Two bit flip flop without merging

A two bit flip flop without merging consist of individual two one bit flip flops. here two different clocks are used .

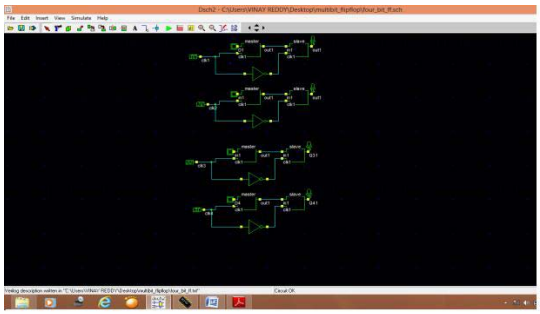


Figure 4: Multi bit flip flop before merging here 4 individual clocks are used

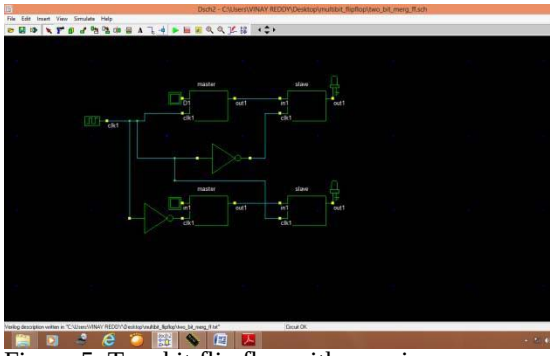


Figure 5: Two bit flip flop with merging

A two bit flipflop with merging is shown in figure. Which consist of only one clock cycle which is reduces the power of the circuit.

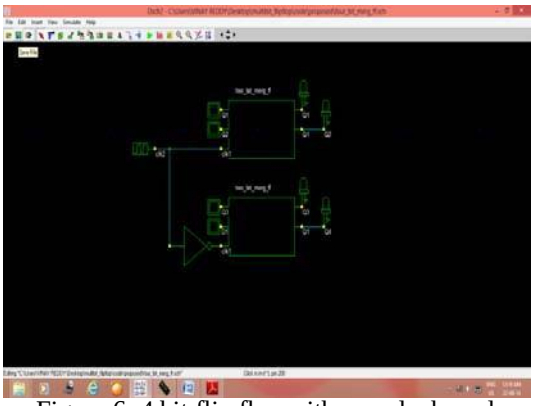


Figure 6: 4 bit flip flop with one clock cycle

III. RESULTS AND ANALYSIS

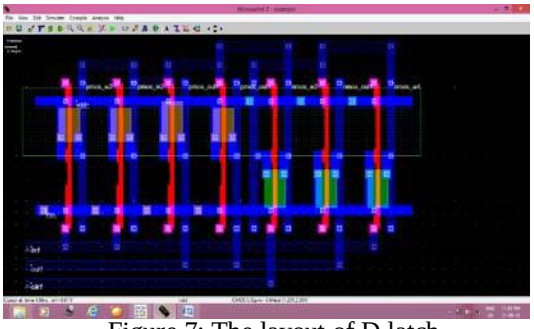


Figure 7: The layout of D latch

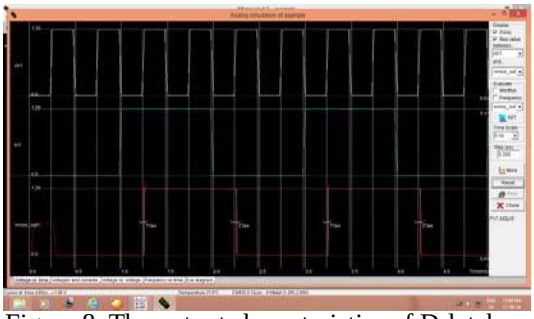


Figure 8: The output characteristics of D-latch for one bit input

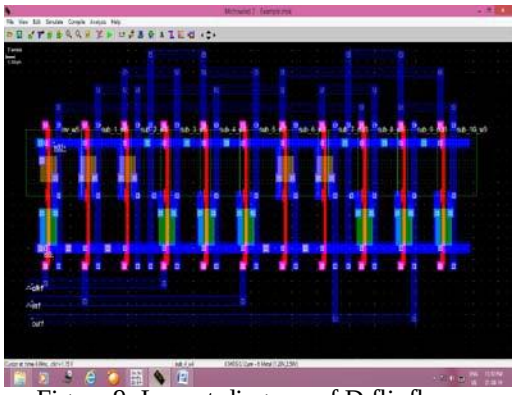


Figure 9: Layout diagram of D flipflop

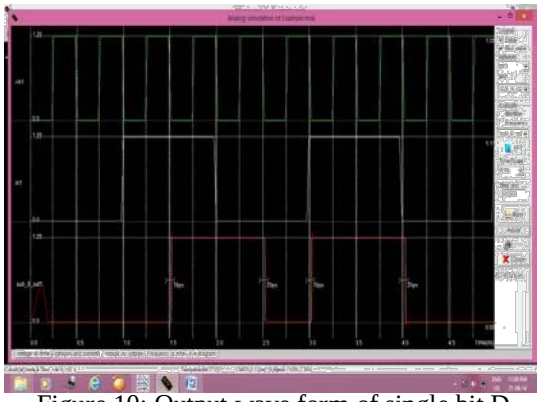


Figure 10: Output wave form of single bit D flipflop

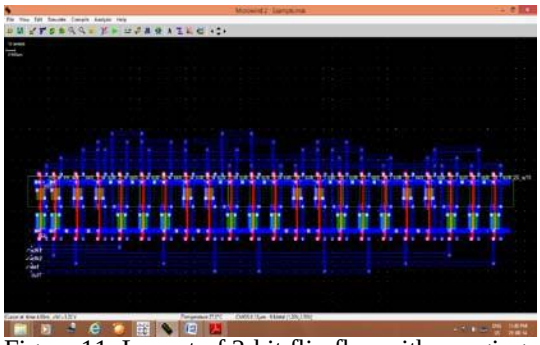


Figure 11: Layout of 2-bit flip flop with merging

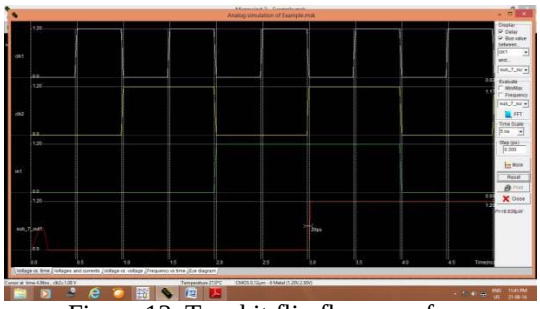


Figure 12: Two bit flip flop waveform

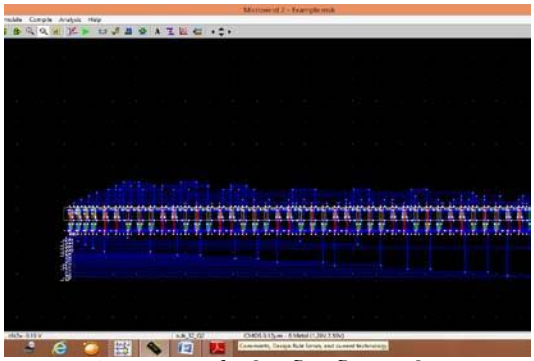


Figure 13: Layout of 4-bit flip flop with merging

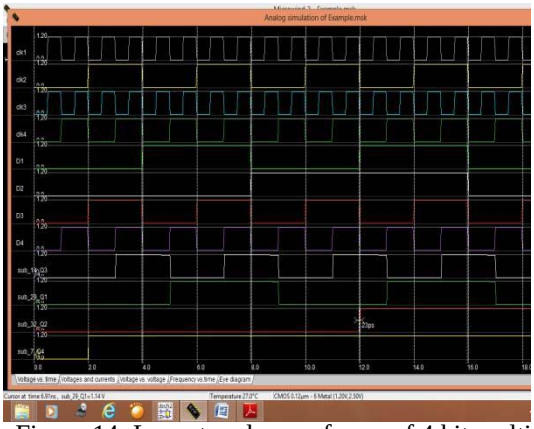


Figure 14: Layout and wave forms of 4 bit multi bit flipflops

V. CONCLUSION

It has been shown that reducing the supply voltage is the most direct means of reducing dissipated power and operating CMOS devices is considered to be the most energy-efficient solution for low-performance applications.

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