Speed Comparison of Various Multipliers

Jyoti Sharma¹, Sachin Kumar²

¹Department of Electronics and Communication Engineering, Meri college of Engineering & Technology, Sampla, Bhadurgarh, Haryana, INDIA
²Assistant Professor, Department of Electronics and Communication Engineering, Meri college of Engineering & Technology, Sampla, Bhadurgarh, Haryana, INDIA

ABSTRACT:

The multiplication operation is an integral part of any digital system or digital computer, most notably in signal processing, graphics and scientific computation. It requires more hardware resources and processing time than addition and subtraction. In fact, 8.72% of all instructions in a typical processing unit is multiplier. The speed of the system depends upon speed of the multiplier to a large extent. This necessitates the need of a high speed multiplier. With the advancement in technology, various techniques have been proposed to design multipliers, which offer high speed, low power consumption and lesser area. Thus making them suitable for various high speed, low power compact VLSI implementations. This paper presents a novel design of a high-speed Hybrid Wallace tree multiplier.

Keywords: Array, Architecture, Digital, Mathematical, Multiplication, Parallel, Serial, Wallace

I. INTRODUCTION

Multiplication is a mathematical operation that at its simplest is an abbreviated process of adding an integer to itself a specified number of times. A number (multiplicand) is added to itself a number of times as specified by another number (multiplier) to form a result (product). The multiplicand is multiplied by each digit of the multiplier beginning with the rightmost, LSD. Intermediate results (partial-products) are placed one atop the other, offset by one digit to align digits of the same weight. The final product is determined by summation of all the partial-products. Multiplication involves three main steps [1]:

- Partial product generation
- Partial product reduction
- Final addition

For the multiplication of an n-bit multiplicand with an m-bit multiplier, m partial products are generated and product formed is n + m bits long.

The multiplier architectures can be generally classified into following categories:

- Serial multiplier
- Parallel multiplier

SERIAL MULTIPLIER

The simplest method to perform multiplication is to add series of partial products. The serial multipliers use a successive addition algorithm. They are simple in structure because both the operands are entered in a serial manner. Therefore, the physical circuit requires less hardware and a minimum amount of chip area. However, the speed Performance of the serial multiplier is due to the operands entered sequentially.
Most advanced digital systems incorporate a parallel multiplication unit to carry out high-speed mathematical operations. A microprocessor requires multipliers in its arithmetic logic unit and a digital signal processing system requires multipliers to implement algorithms such as convolution and filtering. Parallel multipliers [2] present high-speed performance, but are expensive in terms of silicon area and power consumption because in parallel multipliers both the operands are input to the multiplier in parallel manner. Therefore, the circuitry occupies a much larger area and is more complex as compared to serial multipliers.

II. METHODOLOGY

This paper presents a novel design of a high-speed Hybrid Wallace tree multiplier.

The design is implemented using Verilog HDL code and successfully simulated using Xilinx ISE 10.1 Synthesis tool.

III. ARRAY MULTIPLIER

Array multipliers are used with minimum complexity. They are easily Scalable. These are used with pipelined structure. Because of having less complexity they possess regular shapes and easy to place and route. Along with these advantages array multipliers comprise some disadvantages also.

Disadvantages:
- High power consumption
- More digital gates resulting in large chip area

IV. WALLACE TREE MULTIPLIER

A fast process for multiplication of two numbers was developed by Wallace. In 1964, C.S. Wallace [4] observed that it is possible to find a structure, which performs the addition operations in parallel, resulting in...
Wallace introduced a different way of parallel addition of the partial product bits using a tree of carry save adders, which is known as “Wallace Tree” [3]. A Wallace tree is an efficient hardware implementation of a digital circuit that multiplies two integers. In order to perform the multiplication of two numbers with the Wallace method, partial product matrix is reduced to a two-row matrix by using a carry save adder and the remaining two rows are summed using a fast carry-propagate adder to form the product. This advantage becomes more pronounced for multipliers of bigger than 16 bits. WT increases speed because the addition of partial products is now. In WT architecture, all the bits of all of the partial products in each column are added together by a set of counters in parallel without propagating any carries. Another set of counters then reduces this new matrix and so on, until a two-row matrix is generated. Wallace method uses three-steps to process the multiplication operation.

- Formation of bit products.
- The bit product matrix is reduced to a 2-row matrix by using a carry-save adder.
- The remaining two rows are summed using a fast carry-propagate adder to produce the product.

### V. COMPARISON

Generally, it is not possible to say that an exact multiplier yields to greater cost-effectiveness, since trade-off is design and technology dependent. These basic array multipliers consume low power and exhibit good performance, however their use is limited to sixteen bits. Wallace’s strategy for carry save adder trees is to combine the partial product bits as early as possible. This method yields to simpler CSA tree and a wider carry propagate adder and the designs using the Wallace tree method are fast. However a logarithmic depth reduction tree based CSA’s has an irregular structure that makes the design and layout difficult. Moreover connections and signal path of varying length may lead to signal skew that have implications for both power and performance. Comparison of two multipliers is shown in Table 1

<table>
<thead>
<tr>
<th>Multiplier Type</th>
<th>Speed</th>
<th>Circuit Complexity</th>
<th>Layout</th>
<th>Area</th>
</tr>
</thead>
<tbody>
<tr>
<td>Array</td>
<td>Low/Medium</td>
<td>Simple</td>
<td>Regular</td>
<td>Smallest</td>
</tr>
<tr>
<td>Wallace</td>
<td>Higher</td>
<td>Medium</td>
<td>More irregular</td>
<td>Large</td>
</tr>
</tbody>
</table>

Table 1. Comparison between multipliers [5]

### VI. IMPLEMENTATION

Simulation result of 16x16 bit Hybrid Wallace tree multiplier
VII. CONCLUSION

The architecture designs of 16 x16-bit, Hybrid Wallace tree multiplier is done in the paper. The design is implemented using VerilogHDL code and successfully simulated using Xilinx ISE 13.4 Synthesis tool. The computation delay for 16x16 bit hybrid Wallace multiplier is 30.887 ns. The experimental results indicate that Hybrid Wallace multiplier provide 78.41% increase in speed compare to array multiplier. Hence, Hybrid Wallace tree multiplier is used in high-speed application.

REFERENCE