Technique for Designing High Speed Noise Immune CMOS Domino High Fan-in Circuits

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ABSTRACT

Dynamic logic circuits provide more compact designs with faster switching speeds and low power consumption compared with the other CMOS design styles. Domino logic overcomes the difficulties in dynamic circuits such as charge sharing and cascading. In this paper we are proposing a wide fan-in circuit with increased switching speed and noise immunity. Speed is achieved by quickly removing the charge on the dynamic node during evaluation phase, compared to the other circuits. The design also offers less Power Delay Product (PDP). The design is exercised for 20% variation in supply voltage. The design shows a 1.83% improvement in Average Noise Threshold Energy (ANTE). Using the proposed technique an Octal-to-binary encoder is designed and simulated.

Keywords-- CMOS design, Power Delay Product, Average Noise Threshold Energy

I. INTRODUCTION

The rapid advancements in the field of VLSI is due to the increased use of battery operated devices such as laptops, PDAs, mobiles etc., advancements in wireless communications and computations are the urge for low power budgets and compactness. To achieve this, the transistor size has been continually scaled down and to have proper operation of the device, the supply voltages have also been scaled. As the technology aggressively scales down, the density on the chip has increased and hence the interconnection density, which increased the coupling capacitance of the circuit. This lead to increased interaction between the connections and thereby increasing crosstalk and system failures. On the other hand with the decrease in supply, the gate threshold is decreased to preserve system throughput and so leakage currents have increased. And therefore the noise margins of the gate reduced.

Dynamic logic circuits found their wide application in high speed, low power areas such as microprocessors, digital signal processing, dynamic memories etc., because of their low device count, high speed, short circuit power free and glitch free operation [2]. On the other hand it is also possible to design a dynamic logic unit that is smaller than its static counterpart. Dynamic logic consists of pull down network realizing the logic. From the basic theory of dynamic logic the circuit is pre-charged and evaluated at every clock cycle. Due to high clock frequency amount of noise gets induced and power consumption increases. The main draw backs in dynamic logic are charge sharing and cascading. To overcome these problems domino logic is used. When a dynamic gate is cascaded by a static inverter, it is called Domino logic. Domino gates runs faster than the static gates as they present much lower input capacitance for the same output current and a lower switching threshold.

The leakage immunity is of more concern in high fan-in circuits because of larger leakage due to more parallel evaluation paths. Since the leakage current is proportional to the fan-in, the noise immunity decreases with increase in fan-in. Leakage and noise immunity are major issues for the high fan-in domino logic circuits, because the evaluation transistor are all in parallel, leaking the charge from pre-charge node. In this paper we are proposing a technique to reduce power and increase speed and noise immunity of a high fan-in domino gate.

II. PROBLEM STATEMENT

The basic domino logic stage consists of logic realized using N-MOS (Mn) in pull down network and the pull up net work consists of a single P-MOS (Mp) to pre charge the dynamic node to logic high as shown in Fig.1. The dynamic node is cascaded into a static inverter from where the gate output is taken and can be connected to the N-MOS input of the next stage[1]. When clock = 0, the dynamic node charges to Vdd and the bottom transistor Mn is responsible for holding the charge on the dynamic node irrespective of the input combination applied to the pull down network. Thus the output goes to logic 0 during this interval (pre-charge phase). When the clock = 1(evaluation phase) the pre-charge transistor (Mp) goes off, allowing the dynamic node to settle down to a state determined by the inputs . Based on the logic implemented, the charge on the dynamic node may be retained at logic 1, thus output remains at logic 0 or the
dynamic node may get discharged to logic 0 and output may rise to logic 1. During evaluation phase when all the inputs are at logic 0, dynamic node should be at logic 1, but the pull down network leaks the charge stored on the dynamic node due to sub threshold leakage. This is again compensated by P-MOS keeper (Fig 2), which aims to restore the charge on the dynamic node. But when a noise pulse occurs at any of the input such that pull down network provides a direct path to ground, the keeper may not be able to retain the charge on the dynamic node and the node gets wrongly discharged. As the noise in Domino gates is becoming more important than area, power and delay issues in the sub micro meter regime, recently several techniques have been proposed [6],[7] to reduce noise in domino circuits. All the techniques have aimed at reducing the noise effect, but have several drawbacks related to area, power and delay.

III. IMPACT ON POWER CONSUMPTION

Power Consumption Is One Of The Most Important Constraints In The Designing Of Any Dynamic Logic Circuit. Domino Cmos Logic Circuit Family Finds A Wide Variety Of Applications In Microprocessors, Digital Signal Processors, And Dynamic Memory Due To Their High Speed And Low Device Count. However, There Are Inevitable Problems That Degrade The Noise Immunity Of This Family; They Are The Inevitable Leakage Current And The Charge Sharing. Added To The Drawbacks Is The Relatively Large Power Consumption, Especially If Compared To The Static Complementary Cmos Logic Family. To Make The Matter Worse, These Drawbacks Are More Tactile With The Scaling Of Cmos Technology From One Generation To The Next. In This Chapter, The Impact Of Cmos Technology Scaling On The Performance Of Domino Cmos Logic Has Been Investigated.

A simple AND gate is designed using Domino-logic and it is simulated at different technologies.
Fig. 3.3 Basic domino AND gate schematic simulation.

Fig. 3.4 Complete Layout of Basic domino AND gate Schematic.
Fig. 3.5 Basic domino AND gate-Extraction of Layout.

Fig. 3.6 Basic domino AND gate Extraction of Layout-Parasitic components.
After simulating this circuit at different technologies the following observations were made.

### TABLE 3.1 Comparison of parameters with technology for Basic Domino AND Gate.

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<thead>
<tr>
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<tbody>
<tr>
<td>Tsmc 035.mod</td>
<td>3.375</td>
<td>0.549</td>
<td>-0.680</td>
</tr>
<tr>
<td>Tsmc 025.mod</td>
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<td>0.365</td>
<td>-0.562</td>
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<td>Tsmc 018.mod</td>
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<td>0.607</td>
<td>-0.832</td>
</tr>
<tr>
<td>Ami 05.mod</td>
<td>3.276</td>
<td>0.708</td>
<td>-0.918</td>
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From the above table it is observed that with the down scaling of technology, more power is consumed. Specifically, the need to decrease the dynamic power consumption forces us to use a lower power-supply voltage. This in turn necessitates the reduction of threshold voltage to maintain the performance with the associated increase in sub threshold leakage current. So, a properly sized PMOS keeper must be used to compensate for this leakage. It will be found that the speed, which is the major advantage of domino logic compared to other logic styles, will degrade with CMOS technology scaling due to the contention current of the keeper.

### 3.2 PMOS Keeper To Compensate Charge Lost:

However, it has been assumed in the previous paragraph that there is no leakage of the charge stored on the dynamic node capacitor, $CL$. In practice, however, there are various sources of leakage during the evaluation phase even if the input combination does not allow discharging of $CL$. Among these sources are the sub threshold leakages current, the gate tunnelling current, and others. Leakage current is very small but finite. Due to concentration gradient between source and drain terminals of MOSFET, it flows. It is an inevitable problem in dynamic circuits. Also, the charge stored on $CL$ may be shared with one of the drain capacitors associated with one of the NMOS transistors of the PDN for some of the input combinations. So, a PMOS keeper must be used as shown in Fig. 2.8 in order to replenish the charge lost from $CL$, thus maintaining the noise margin at an acceptable level. However, during the evaluation phase, if $CL$ is to discharge through the PDN, the contention current from the keeper will slow down the discharging process. So, this keeper must be weak.
Fig. 2.9 Basic domino AND gate-using PMOS-keeper schematic implementation.

Fig. 3.10 Basic domino AND gate-using PMOS-keeper schematic simulation.
After simulating this circuit at different technologies the following observations were made.

**TABLE 3.2** Comparison of parameters with technology for Basic Domino AND Gate using PMOS Keeper.

<table>
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<tr>
<td>Ami 12.mod</td>
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<td>Ami 05.mod</td>
<td>21.880</td>
<td>0.708</td>
<td>-0.918</td>
</tr>
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</table>

**IV. COMPILER**

4.1. Domino NAND and AND gate
Domino NOR and OR gates output waveforms
4.2. Domino logic 4 input OR gate

Output waveform of Domino logic 4 input OR gate

4.3 Domino diode footed OR gate
4.4 Domino scheme 8 OR logic

Domino diode footed OR gate output waveform

Domino scheme 8 OR logic output waveform
4.5. Proposed scheme OR logic

Domino proposed scheme OR logic output waveform
V. CONCLUSION AND FUTURE SCOPE

In this paper we have proposed high speed low PDP domino logic circuit, which exhibits some noise tolerance at the output node. Simulations are done using Tanner T-Spice with PTM 16nm low power technology files. From the results it is proved that the proposed design is better than the previous designs and offers about 29% reduction in delay and 3.5% reduction in PDP is achieved. Average Noise Threshold Energy (ANTE) is calculated and found an increase of 1.83% in ANTE. An octal-to-
binary encoder is designed and simulated with proposed technique.

REFERENCES