

## Watermarking in Ycber Channel using XILINX System Generator

Samadhan G Rupnar<sup>1</sup>, S. S. Agrawal<sup>2</sup>

<sup>1</sup>P.G. Student, Department of Electronics and Telecommunication Engineering, Government College of Engineering, Aurangabad, Maharashtra INDIA

<sup>2</sup>Assistant Professor, Department of Electronics and Telecommunication Engineering, Government College of Engineering, Aurangabad, Maharashtra INDIA

### ABSTRACT

This paper aims to present a technique of watermarking in YCbCr channel. The system is implemented using Xilinx System Generator. It presents the architecture for watermarking in different components (Y, Cb and Cr) in YCbCr channel. Water marking in different components is tested for various images and watermark is extracted. Original watermark and extracted watermark are analyzed and compared. The design is implemented targeting Virtex 5 (VC5V5X50t-1ff1136) device.

**Keywords** –Color Space Conversion, PGA, Watermarking, Xilinx System Generator.

components are added together to form a desired color and are represented by a three dimensional, Cartesian coordinate system as shown in Figure 1.

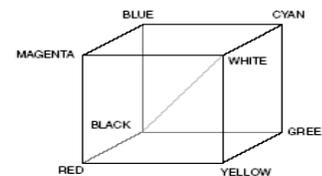


Figure 1: RGB Color Cube

## I. INTRODUCTION

### 1. Color Space Conversion

A color is specified using three coordinates, or parameters. The position of the color within the color space is described by these parameters. These parameters do not describe what the color is, that is dependent on which color space is being used. A color space is a mathematical representation of a set of colors.

The most popular color models are:

- i. RGB (used in computer graphics).
- ii. YIQ, YUV, YCbCr (used in video systems).
- iii. CMYK (used in color printing).

However, these color spaces are not directly related to the insightful ideas of hue, saturation, and brightness. All color spaces can be derived from the RGB information supplied by devices such as cameras and scanners.

The red, green and blue (RGB) color space is extensively used all over computer graphics. Red, green and blue are three primary additive colors; individual

The RGB color space is the most widespread choice for computer graphics, because color displays uses red, green, and blue to create the desired color. The RGB color model colors, as shown in Figure 2 can be written in several different ways. Y is defined to have a range of 16–235; Cb and Cr are defined to have a nominal range of 16–240.

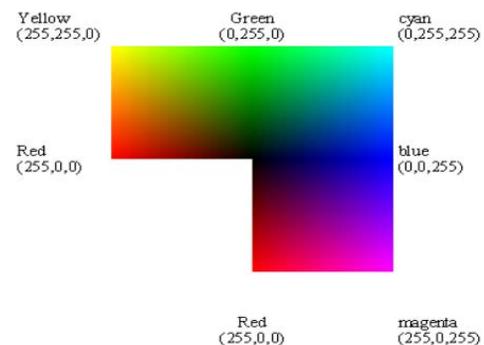


Figure 2: RGB Color model

Color space conversion is an important part of image processing and transmission. The images are stored in RGB color space [1]. As bandwidth requirement of images in RGB color space is very large, it is impracticable to transmit it. Therefore, RGB color space is converted into other color space such as YUV, YIQ and YCbCr to overcome this problem. The YCbCr color space is a scaled and an offset kind of the YUV color space.

The color space is dependent on the application and the requirement such as bandwidth, computation and storage in analog or digital domains [2]. In this paper the architecture of watermarking in YCbCr channel is presented for efficient implementation using Field Programmable Gate Array (FPGA) platform. YCbCr color model is a chroma model of CCIR.601 coding mode, which is widely used in color display of TV. Y denotes the luminance component in this color space and it shows the brightness. Both Cb and Cr represent the chrominance components. The YCbCr color space is selected for following reasons [3]. The luminance component (Y) can be adopted to solve the problem of illumination variation and it is easy to program because of its color independency. According to [4], in YCbCr color space; the skin color cluster is more compact than in other color spaces. YCbCr color space has the smallest overlap between skin and non-skin information under different illumination conditions. YCbCr color space is very important in video compression standards (e.g. MPEG and JPEG) [5]. Video systems use YCbCr color space, one of the families of color spaces. ITU-R BT.601 standard defines YCbCr color space for standard-definition television used in digital component video. RGB color space along with YCbCr color space are two primary color spaces used to characterize digital component video.

Prathibha et al. [6] have proposed the color space converter module for changing the image from RGB color space to YCbCr color space. The color space conversion module was designed using VHDL and was implemented on an FPGA.

## 2. Watermarking

Watermarking is the process of hiding a predefined logo or pattern into multimedia like image, audio or video in such a way that quality and imperceptibility of media is preserved. Predefined logo or pattern represents identity of a creator or rights. In recent years, rapid growth in digital multimedia has been observed. Digital information (image, audio, and video) is sent through Internet without much effort and money. But, in digital multimedia security is the main issue. Due to these remarkable changes, the entertainment industry has to adopt the technologies that allow it to retain the copyright controls provided by the law and bind the new world to increase the industry size and augment the consumer experience.

The implementation of the design could be on many platforms such as software, hardware, embedded

controller, DSP, etc. System performance is a major parameter while designing complex systems. The standard DSP which has Von Neumann style of fetch-operate-write back computation fails to exploit the inherent parallelism in the algorithm. Thus, high throughput requirements of real-time digital systems often dictate hardware exhaustive solutions. FPGAs provide a rapid prototyping platform. They can be reprogrammed to accomplish different functionalities without incurring the non-recurring engineering costs naturally associated with custom IC fabrication.

Watermarking algorithm was implemented by Korrapati et al. [7] on FPGA platform. Hardware architecture of watermarking was realized using the Xilinx Block Sets available in Simulink. The generated Hardware Co-Simulation was tested on the FPGA development board. Validation was done in terms of area, power and performance metrics. Amit Joshi et al. [8] proposed watermarking algorithm for real time image and video processing. It has combined approaches of spatial and frequency domain and it has overcome block artifact problem of DCT.

Mehdi Khalili [9] has proposed a Novel Secure, Imperceptible and robust CDMA Digital Image Watermarking in JPEG-YCBCR channel using DWT2.

In this paper the host image is converted into JPEG-YCbCr channels; then the Y channel is decomposed into wavelet coefficients. For more security of watermark, the watermark W is converted to a sequence and then a random binary sequence R of size n is adopted to encrypt the watermark.

## 3. Xilinx System Generator Design Flow

In the industrial applications and in our daily life image processing and computer vision methods have become increasingly significant. Image processing usually matches tasks with very high computational requirements. The standard processors and computers or computers connected to the computational network can handle such tasks [10]. However, this type of approach is standalone. Specialized hardware solutions based on digital signal processors (DSP) or a FPGA are usually used in embedded systems. Xilinx System Generator allows the design of hardware system starting from a graphical high level Simulink environment. Xilinx System Generator outspreads the conventional Hardware Description Language (HDL) design providing graphical modules, and thus does not require a detailed knowledge of this complex language. The Simulink graphical language allows an idea of the design through the use of available Xilinx System Generator blocks and subsystems. It decreases the time crucial between the detailed control design and can be easily implemented on hardware. The software facilitates for the hardware simulation and hardware-in-the-loop verification, referred to as hardware co-simulation, from within this environment. This methodology provides easier

hardware verification and implementation compared to HDL based approach [11].

For commercial applications like video recording, video surveillance, movie production, where a real-time response is important, software solution is not recommended due to its long time delay. FPGAs have advantages in both fast processing speed and field programmability, therefore an FPGA is the best approach to build a module for verifying design concepts and performance. Figure 3 outlines the flow of design using Xilinx System Generator.

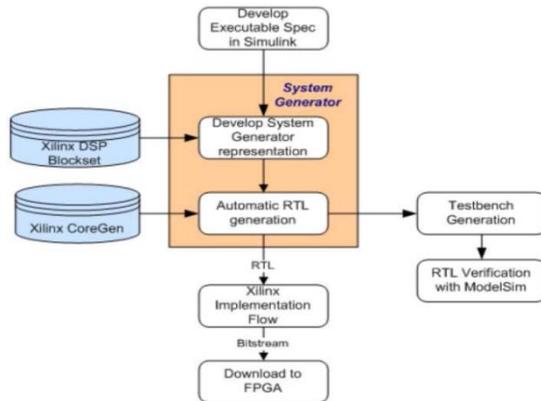


Figure 3: Xilinx System Generator Design Flow

## II. SYSTEM DESIGN

The block diagram for the proposed system is shown in Figure 4. The system consists of color space conversion (RGB to YCbCr, YCbCr to RGB) and watermark embedding in one of the components of Y or Cb or Cr architecture using Xilinx System Generator.

Original Image and Watermark image are read through 'Image From File' block available in computer vision toolbox of Simulink. Then these images are converted into 1D array before applying as input to Xilinx blocks through Gateway In. Color space conversion is carried out. Watermark embedding is carried out in one of the components i.e. Y or Cb or Cr. Salt & Pepper, Median Filtering attacks are applied to watermark embedding algorithm. Extraction of watermark is accomplished and performance evaluation is done through the workspace. This design helps us to reduce the overall hardware requirement of the system.

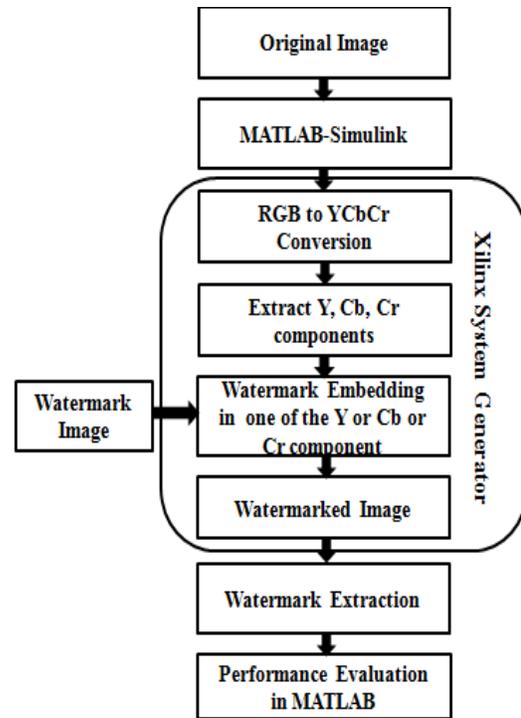


Figure 4: Block Diagram of Proposed System

The following equations have been used to generate the logic used in the color conversion module.

$$Y = 0.299R + 0.587G + 0.114B + 16$$

$$Cb = -0.169R - 0.331G + 0.5B + 128$$

$$Cr = 0.5R - 0.419G - 0.081B + 128$$

AND

$$R = Y + 1.403(Cr - 128)$$

$$G = Y - 0.344(Cb - 128) - 0.714(Cr - 128)$$

$$B = Y + 1.772(Cb - 128)$$

The watermark embedding architecture is given in Figure 5.

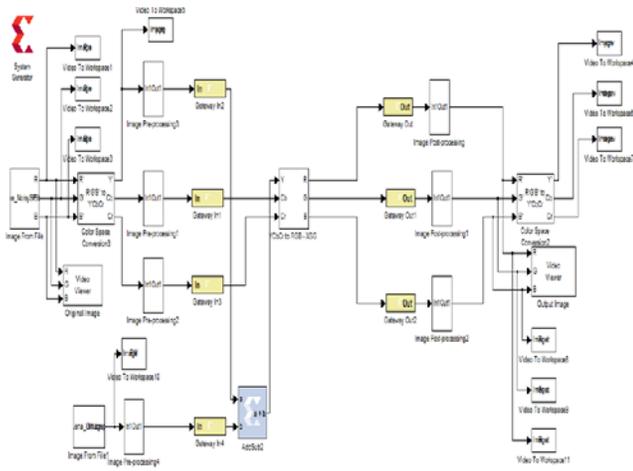


Figure 5: Watermark embedding architecture

Figure 6 shows the RGB to Y conversion. The values of R, G and B are read through Gateway In. Computation is done as per given formula and output is presented for video display and analysis through Gateway Out and Image Post Processing interface in Simulink.

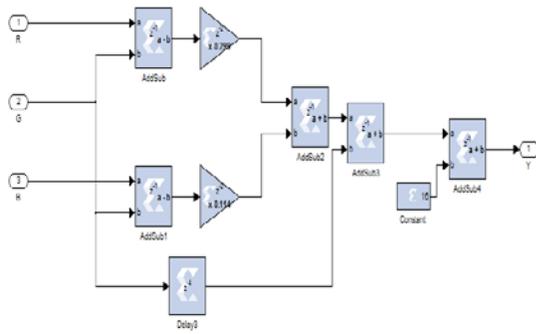


Figure 6: RGB to Y conversion

Figure 7 and Figure 8 represent the RGB to Cb conversion and RGB to Cr conversion respectively. The computation is done as per given formulae and result is given to video display.

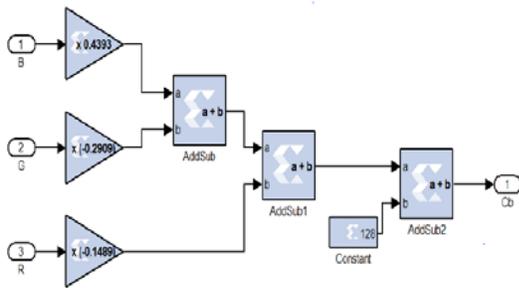


Figure 7: RGB to Cb conversion

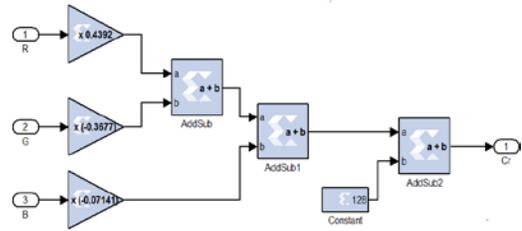


Figure 8: RGB to Cr conversion

### III. IMPLEMENTATION

#### 1. Hardware Co-Simulation

The important feature of Xilinx System Generator is Hardware Co-Simulation or the Hardware in the loop. By connecting the FPGA board using JTAG or Ethernet interface with PC the design is verified in the hardware as well as in the software environment and comparison becomes straightforward as both the results are available simultaneously side by side. Figure 9 shows the architecture of Hardware Co-Simulation.

This feature gives the user flexibility for the changes required to be done for correction, enhancement, up gradation, etc without wastage of time, money and the resources required.

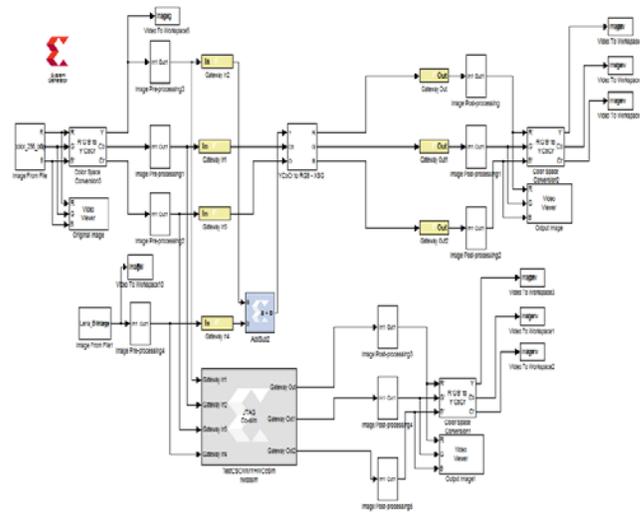


Figure 9: Architecture of Hardware Co-Simulation

The compilation configuration of Xilinx System Generator is given in Figure 10. The target hardware selected is Virtex5-ML506. The compiled files are stored in the Target Directory specified. Clocking for Simulink and for FPGA board is specified.

By clicking generate button the compilation is started and the Hardware co-simulation block with appropriate inputs and outputs are generated in the library.

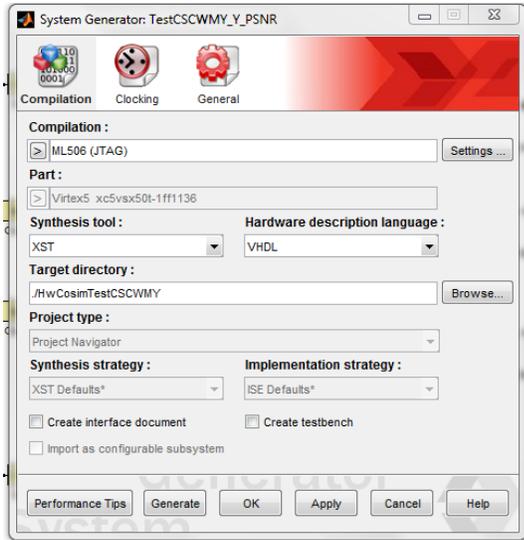


Figure 10: Xilinx System Generator configuration

2. Resource Utilization

The system is implemented on Virtex5 device ML506 and Resource Utilization of this device is given in Table 1. It is observed that LUT-FF pair and Bonded IOBs have the maximum utilization among all available resources.

Table 1: Resource Utilization

Sr No	Logic Devices	Virtex 5 – ML506		
		Used	Available	%
1	LUT-FF Pair	919	1512	60.78
2	Bonded IOBs	271	480	56.45
3	Occupied Slices	492	8160	6.02
4	Slice LUTs	1424	32640	4.36
5	Slice Registers	1007	32640	3.08

3. Power and Temperature analysis

Power and Temperature analysis for the device Virtex5-ML506 is given in Figure 11.

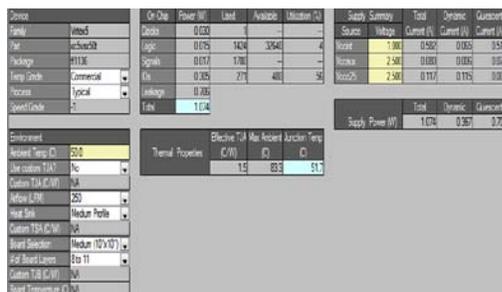


Figure 11: Power and Temperature Analysis

Total power consumption of the proposed system

for Virtex5-ML506 is 1.074w, junction temperature is 51.7° C and maximum ambient temperature is 83.3° C. The maximum frequency of operation for ML506 device is 113.520 MHz.

IV. PERFORMANCE EVALUATION



1. Peak Signal To Noise Ratio (PSNR)

The term PSNR is an expression for the ratio between the maximum possible value (power) of a signal and the power of distorting noise that affects the quality of its representation. PSNR is expressed in terms of the logarithmic decibel scale.

PSNR values for various watermarked images are given in Table 2.

Table 2: PSNR values of Watermarked images

Sr No	Input Image (Color)	Watermark addition in Y	Watermark addition in Cb	Watermark addition in Cr
		PSNR(dB)	PSNR(dB)	PSNR(dB)
1	Lena	51.0892	49.8387	48.8723
2	Peppers	51.0397	49.8383	48.9299
3	Mandrill	51.0184	49.7091	48.8965
4	House	51.0884	49.7441	48.8744

Images are attacked with Salt & Pepper and Median Filter. PSNR calculation is carried out through workspace variables and given in Table 3.

Table 3: PSNR values with different attacks

Sr No	Image	Watermark addition in Y		Watermark addition in Cb		Watermark addition in Cr	
		S&P Noise	Med Filter	S&P Noise	Med Filter	S&P Noise	Med Filter
		PSNR	PSNR	PSNR	PSNR	PSNR	PSNR
1	Lena	22.1246	28.4544	22.1170	28.4002	22.1242	28.3691
2	Peppers	22.0111	28.8255	22.0053	28.8331	22.0142	28.2936
3	Mandrill	22.3444	23.0072	22.3408	23.0062	22.3440	23.0019
4	House	22.2828	29.4256	22.2782	29.4133	22.2796	29.4135

## 2. Correlation Value

Correlation values define the closeness between Original watermark and Extracted watermark. Table 4 shows correlation values between Original watermark and Extracted watermark for different attacks.

Table 4: Correlation values between Original Watermark and Extracted Watermark for different Noise attacks.

Sr No	Image	Watermark addition in Y		Watermark addition in Cb		Watermark addition in Cr	
		S&P Noise	Med Filter	S&P Noise	Med Filter	S&P Noise	Med Filter
		Correlation Value	Correlation Value	Correlation Value	Correlation Value	Correlation Value	Correlation Value
1	Lena	0.9913	1	0.9903	1	0.9899	1
2	Peppers	0.9909	1	0.9896	0.9992	0.9797	0.9923
3	Mandrill	0.9914	1	0.9898	1	0.9906	1
4	House	0.9920	1	0.9907	1	0.9887	0.9887

From the PSNR values and correlation values with attacks it is observed that the watermark embedding in Y component is less susceptible than watermark embedding in the components Cb or Cr.

## V. FUTURE SCOPE

The system is implemented in FPGA device and it can be implemented as an embedded system. After design finalization it can be implemented as System On Chip (SoC) which will be easy to be incorporated in portable systems and handheld devices.

## VI. APPLICATIONS

The system can be utilized in following applications

1. Video Conferencing
2. Telemedicine
3. Video Processing
4. TV Broadcasting
5. Industrial Trainings.

## VIII. CONCLUSION

With this design approach the distinctive features of using programmable digital devices are reached. Repeating a design consists in reprogramming the FPGA in the chosen board. The design and simulation times are decreased; as a result the time to market is minimized. The used tool gives great flexibility i.e. the design parameters can be changed and new features can be checked within few minutes.

Xilinx system generator is a very handy tool for developing computer vision algorithms. It can be described as a timely, valuable option for developing in a contented way than that permitted by Hardware Description Languages,

It is concluded that watermarking in color space conversion in Xilinx System Generator for Y component gives better results with flexibility and saves development time and cost compared to watermark embedding in component Cb or Cr.

## REFERENCES

- [1] Keith Jack, Video Demystified: A Handbook for the Digital Engineer, LLH Technology Publishing, Third Edition, 2001.
- [2] F. Bensaali, A. Amira and A. Bouridance, "Accelerating matrix product on reconfigurable hardware for image processing applications", IEE Proceedings on Circuits and Devices Systems, vol. 152, No. 3, June 2005
- [3] Chiunhsiun Lin, "Face detection in complicated backgrounds and different illumination conditions by using YCbCr color space and neural network." Elsevier, Pattern Recognition Letters 28 (2007), pp. 2190–2200, July 2007.
- [4] X. Xia, C. Boncelet, and G. Arce, "A Multiresolution Watermark for Digital Images." Proc. IEEE Int. Conf. on Image Processing, vol. I, pp. 548-551, Oct. 1997.

- [5] Garcia, C., Tziritas, G., "Face detection using quantized skin color regions merging and wavelet packet analysis." IEEE Trans. Multimedia, 1 (3), pp. 264–277, 1999.
- [6] E. Prathibha, Dr.A.Manjunath, Likitha.R "RGB to YCbCr Color Conversion using VHDL approach"International Journal of Engineering Research and Development,vol-1,issue-3, June 2012
- [7] Korrapati Rajitha1, Usha Rani.Nelakuditi1, Venkata Naresh Mandhala,"FPGA Implementation of Watermarking Scheme Using XSG"International Journal of Security and Its Applications,Vol 9,2015
- [8] Prachi V. Powar, S.S. Agrawal "Implementation of Digital Video Watermarking Scheme Based On FPGA" International Journal of Electrical, Electronics and Computer Systems (IJEECS), Vol-1, 2013
- [9] Amit Joshi, Vivekanand Mishra and R. M. Patrikar "Real Time Implementation of Digital Watermarking Algorithm for Image and Video Application"
- [10] Mehdi Khalili "A Novel Secure, Imperceptible and robust CDMA Digital Image Watermarking in JPEG-YCBCR channel using DWT2"
- [11] Inc., T. M.: Embedded mark Language User Guide. The MathWorks Inc., 2007
- [12] Xilinx System Generator User's Guide, www.Xilinx.com.