Low Power Memory Design Using Source Coupled Logic

Alina¹, Sachin Kumar²

¹Department of ECE, Meri College of Engineering & Technology, Sampla, Bhiwani, Haryana, INDIA
²Assistant Professor, Department of ECE, Meri College of Engineering & Technology, Sampla, Bhiwani, Haryana, INDIA

ABSTRACT

Design flexibility and power consumption in addition to the cost, have always been the most important issues in design of integrated circuits. Power dissipation and energy consumption are especially important when there is a limited amount of power budget or limited source of energy. Recently advances in VLSI Technology have made it possible to put a complete System on Chip (SOC) which facilitates the development of PDAs, laptop, cellular phones etc. The evolutions of these applications profiles power dissipation as a critical parameter in digital VLSI design.

Source coupled logic (SCL) applications are another examples where power dissipation is the primary design issue. The objective of this paper is “Low power memory design using source coupled logic”. In this paper, the detailed working operation of the memory architecture has been analyzed. The Memory cell design is implemented in 0.18 micron CMOS process technology in both schematic mode and symbol mode. After implementing the memory cell, power analysis by varying parameters like temperature, supply voltage, capacitance and frequency has been done.

Keywords--- CMOS, Integrated circuit, Dynamic power, NMOS, Static power, VLSI.

I. INTRODUCTION

Design flexibility and power consumption in addition to the cost, have always been the most important issues in design of integrated circuits (ICs).

Power dissipation and energy consumption are especially important when there is a limited amount of power budget or limited source of energy. Very common examples are portable systems where the battery life time depends on system power consumption. Many different techniques have been developed to reduce or manage the circuit power consumption in this type of systems. Design flexibility is the other important issue in modern integrated systems. There are many applications requiring integrated systems with reconfigurable characteristics. This property enables users to employ a system at different applications or at different situations without significant extra cost.

In some designs, re-configurability is considered as the main specification of a system. For example, to optimize the power consumption versus frequency of operation, a system should bear a very wide tuning range. In such systems, power consumption is adjusted with respect to the operating frequency in a very wide range.

Low power design reduces cooling cost and increases reliability especially for high density systems. Moreover, it reduces the weight and size of portable devices. The power dissipation in CMOS circuits consists of static and dynamic components. Since dynamic power is proportional to \( V^2 \) and static power is proportional to \( V_{th} \), lowering the supply voltage and device dimensions, the transistor threshold voltage also has to be scaled down to achieve the required performance[1]. Due to the exponential nature of leakage current in sub-threshold region of the transistor, the leakage current can no longer be ignored. In this paper we have been proposed the new CMOS library for the complex digital design using scaling the supply voltage and device dimensions and also suggest the methods to control the leakage current to obtain the minimum power dissipation at optimum value of supply voltage and transistor threshold.

Power dissipation in CMOS digital circuits is categorized into two types[3]: peak power and average power. Peak power affects both circuit lifetime and performance. Average power dissipation is significant for calculating the battery weight and lifetime. Average power is categorized into: dynamic power and static power dissipation. Dynamic power is the component proportional to the operating frequency of the circuit or the frequency of the node switching so it is more important during the normal operations whereas the static power is independent of the frequency so it is more important for battery operated devices.

In case of static power the power is consumed during the steady state condition i.e. when there are no input/output transitions.
In this paper, a new topology for implementing digital circuits for ultralow power applications will be presented. For this purpose, a novel approach for implementing source-coupled logic (SCL) circuits biased in sub threshold regime will be described. In this topology, the speed of operation does not depend on supply voltage and threshold voltage of devices. In addition, the current consumption of each cell can be controlled very precisely down to few Pico-Ampere. Therefore, it is possible to reduce the system power consumption well below the sub threshold leakage current of conventional CMOS circuits.

II. PRIOR APPROACH

Power and cost efficiency, flexibility, performance, and reliability of signal processing in digital domain have promoted designers to gradually replace the traditional analog domain signal processing with the signal processing in digital domain. To improve the speed and implement more complex digital systems, CMOS technology has been continuously scaled down for the past few decades. Technology scaling, however, has made some of the secondary non-ideal effects in CMOS devices more pronounced[2]. Among them, increase of device leakage current is a very important issue for digital circuits. While the static power dissipation of digital CMOS integrated circuits implemented in conventional technologies has been negligible, device leakage current in deep-sub-micron CMOS technologies increases the static power considerably and hence reducing power efficiency.

III. OUR APPROACH

In this paper, a new topology for implementing digital circuits for ultralow power applications is presented. For this purpose, a novel approach for implementing source-coupled logic (SCL) circuits biased in sub threshold regime is described. In this topology, the speed of operation does not depend on supply voltage and threshold voltage of devices. This property, relaxes the design trade-offs in ULP implementations.

3.1 Source Coupled Logic

In SCL, the current consumption of each cell can be controlled very precisely down to few Pico-Ampere. Therefore, it is possible to reduce the system power consumption well below the sub threshold leakage current of conventional CMOS circuits.

3.2 Circuit Topology

The core of an SCL circuit is constructed based on NMOS differential pairs[4]. The logic operation in SCL topology takes place in current domain and hence this type of logic circuits can inherently be very fast. Input and output voltages as well as the steered current, all are a differential signal which is a key characteristic for reducing switching noise.

3.3 Strong Inversion Operation

Assuming that the devices are in SI and using EKV model, the differential output current, \( \Delta I \), can be calculated versus differential input voltage, \( \Delta V_{IN} \).

\[
\frac{\Delta I}{I_{SS}} = \sqrt{2} \cdot \frac{\Delta V_{IN}}{V_t} \cdot \sqrt{1 - \frac{\Delta V_{IN}^2}{2V_t^2}}
\]

Where \( V_t = \sqrt{2I_{SS}n_t \beta} \) denotes the voltage threshold for current switching in differential pair devices.

3.4 Weak Inversion Operation

On the other hand, when the devices are pushed towards WI region, transconductance and differential output currents can be calculated by

\[
G_m = \frac{\frac{\Delta V_{IN}}{2n_t U_T}}{\cosh^2\left(\frac{\Delta V_{IN}}{2n_t U_T}\right)}
\]

Where \( G_m = I_{SS} / (2n_t U_T) \) and

\[
\frac{\Delta I}{I_{SS}} = \tanh\left(\frac{G_m \Delta V_{IN}}{I_{SS}}\right) = \tanh\left(\frac{\Delta V_{IN}}{2n_t U_T}\right)
\]

(3.12)

Operating in sub threshold regime, the device transconductance strongly depends on temperature through \( U_T \), while it does not depend on device sizes. Therefore, it is not possible to change the transfer curve by design parameters.

3.5 Ultra-Low-Power Source-Coupled Logic

In this work, some new techniques for implementing ULP SCL circuits are developed. The main goal is to study the possibility of using CMOS leakage...
current (which is unavoidable in CMOS topology) for successful logic operation in SCL topology. This requires biasing SCL circuits deeply in sub threshold regime and hence implementing sub threshold SCL (STSCL) circuits.

IV. IMPLEMENTATION

The logic function in STSCL circuits is realized by an N-level NMOS switching network. This network can be modelled by a Binary Decision Diagrams (BDD). All possible N-level BDDs topologies are called footprints. A 1-level network can only be mapped to the Buffer and Inverter gates while for networks of 1–3 levels, 19 unique footprints exist and can be mapped to a large number of cells like XOR3, AND3, etc.

One of the main issues in design of standard cell libraries is the area of the cells. Larger cell area not only results in larger chip size, but can also cause speed reduction. Therefore, it is necessary to reduce the size of each cell as much as possible.

One important issue with the STSCL logic cells is that driving strength can be scaled only by scaling the tail bias current. Therefore, for a cell with driving strength of N the size of tail bias NMOS transistor needs to be N times larger than a cell with unit driving strength.

V. SIMULATION RESULTS

Various Analyses on STSCL Inverter:
Power at different Channel Length

At Length = 180nm

Fig. 2. VDD v/s Power at L =180nm

At Length = 150nm

Fig. 3. VDD v/s Power at L =150nm

At Length = 120nm

Fig. 4. VDD v/s Power at L =120nm

Fig. 5. Temperature v/s Power at different length
VI. CONCLUSION

In this paper, the potentials of sub threshold MOS devices for implementing power-performance scalable integrated systems have been studied.

The comparison of CMOS gates & STSCL gates has also been done which shows that power dissipation of SCL gates are far less than CMOS gates, the corner analysis also proves that the SCL gates are fast if right current biasing is done as it is also being a dependent parameter for power dissipation. The other important analyses that are not possible with the Mentor Graphic IC station is power with frequency variation, which according to theory states that the power is independent of frequency variation in SCL technique.

REFERENCE