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Design and Implementation of Low Power High Speed Symmetric Decoder Structure for SDR Applications

Nidhin Sani[1], Agath Martin[2], Abin John Joseph[3] and Nishanth R.[4]
[1]Assistant Professor, Department of Information Technology, CUSAT/CUCEK, INDIA
[2]Assistant Professor, Department of Information Technology, CUSAT/CUCEK, INDIA
[3]Assistant Professor, Department of Electronics & Communication Engineering, CUSAT/CUCEK, INDIA
[4]Assistant Professor, Department of Electronics & Communication Engineering, CUSAT/CUCEK, INDIA

[4]Corresponding Author: nishanth.jino@gmil.com

ABSTRACT

The key objective of this project is to design a decoder which can be used for hardware purposes. Hardware, here accompanies with software which is more we can discuss as a Software Defined Radio application. The decoder implemented here offers to new radio equipment (SDR), the flexibility of a programmable system. Nowadays, the behavior of a communication system can be modified by simply changing its software. Large tree decoder is made by reusing smaller similar sub-modules. Thus the structure is symmetric. The symmetric and regular structure of tree decoder makes the system a less complexity one. The structure obeys regularity and modularity concepts of VLSI circuit, thus is easy to fabricate using cell library elements. Design a Tree Decoder proposed architecture for SDR application on FPGA. The Structures made here are hardware synthesizable on FPGA board and are done in a respective manner. The design to be implementing by using Verilog-HDL language. The Simulation and Synthesis by using Xilinx Vivado design suite.

Keywords-- Software Defined Radio(SDR), Tree Decoder, FPGA, HDL

I. INTRODUCTION

In any communication network, Transmitter and receiverare the two common parts of the system.Decoders are used in the receiver section which is helpful in obtaining the desired information effectively. A decoder takes the coded info from a receive message and changes it into recognizable kind. A decoder is a combinational circuit that converts binary information from n input lines to a maximum of $m=2^n$ output lines. Design of a high performance and efficient static, dynamic and tree decoder is very important for design of a frequency allocator but the main point is to allocate the specified band to assign a set of inputs which is then obtained at the desired output, thus the developing of a reliable and fast frequency allocator is a big problem in itself. A software-defined radio system, or SDR, is a radio communication system where components that have been typically implemented in hardware (e.g. mixers, filters, amplifiers, modulators/demodulators detectors, etc.) square measure instead enforced by means that of software package on a private pc or embedded system. SDR needs to be reconfigurable to address the needs of flexibility and adaptability of SDRapplications.

SDR stands for Software Defined Radio; it's a radio communication system and the parts that are usually implemented in hardware (e.g. detectors, filters, amplifiers, modulators/demodulators, mixers etc.) are instead implemented by means of software on the computer or embedded system. Since the content of SDR isn't new, the rapidly evolving capabilities of digital electronics render practical many processes which used to be only theoretically possible.The SDR and the technologies required for the design and implementation of tree decoder are discussed and the information related to them are presented, the information related to the software language VHDL and simulation and Analysis tools like Xilinx Vivado design suite is presented.A basic SDR system might carries with it a private pc equipped with a sound card, or other analog-to-digital converter, receded by some form of RF front end.Significant amounts of signal process are processed by the general processor, rather than being done in special-purpose hardware (electronic circuits).Such a style produces a radio which may receive and transmit wide completely different radio protocols (sometimes remarked as waveforms) based only on the software used. Software radios have important utility for the military and mobile phone services, both of which must serve a wide variety of changing radio protocols in real time.In the long term, software-defined radios are expected by proponents like the SDR Forum (now The Wireless Innovation Forum) to become the dominant technology in radio communications. SDRs, together with software defined antennas are the enablers of the cognitive radio.

II. LITERATURE REVIEW

Compression is useful technique in digital system, as it reduces the channel bandwidths and storage size. Thispaper presents new Huffman decoder based on binary tree method for improving usage of memory and

speed. It has shown through experiment result related to computational speed that the propose method is superior to otherpredecessor. The customized Huffman hardware decoder comparison is presented at different speed on various FPGA's [5]. Future mobile and wireless communication networks require flexible modem architectures to support the services between differentnetwork standards. Hence, a common hardware platform that can support multiple protocols implemented or controlled by software, generallyreferred to as software defined radio (SDR), is essential. This paper presents a family of dynamically reconfigurable application specific instructionset processors (ASIPs) for channel coding in wireless communication systems. As a weekly programmable intellectual property (IP)core, it can implement by trellisbased channel decoding in a SDR environment. It features binary convolutional decoding, and turbo decoding forbinary as well as duobinary turbo codes for all current and upcoming standards. The ASIP consists of a specialized pipeline with 15 stages and adedicated communication and memory infrastructure. Logic synthesis revealed a maximum clock frequency of 400 MHz and an area of 0.11 mm2for the processor's logic using a low power 65nm technology. Memories require another 0.31 mm^2. Simulation results for Viterbi and turbodecoding demonstrate maximum throughput of 196 and 34 Mb/s, respectively. The ASIP hence outperforms state ofthe art decoder architecturestargeting software defined radio by at least a factor of three while consuming only 60% or less of the logic area[3].

III. PROPOSED METHOD

Big tree decoder can be designed by reusing smaller similar sub-modules. Thus the structure becomes symmetric. The symmetric and regular structure of tree decoder makes the system easy to design. The structure obeys regularity and modularity concepts of VLSI circuit, thus is easy to fabricate using cell library elements. Tree structure requires fewer components with better area and delay optimization.

Design of 4 to 16 tree decoder:

4 inputs given as: A0, A1, B1, B2
1 enable input: Enable
16 output stages: Z0 , Z1 , Z2 , Z3 , Z4 , Z5 , Z6 , Z7 , Z8 , Z9 ,Z10, Z11 , Z12 , Z13 , Z14 , Z15

It is composed of five number 2 to 4 decoders. The input to 4 to 16 decoder is divided into two equal halves and each half is named accordingly.
i.e. X = (Xleft + Xright)
where, Xleft = (B2 ,B1) and Xright = (A1 , A0)

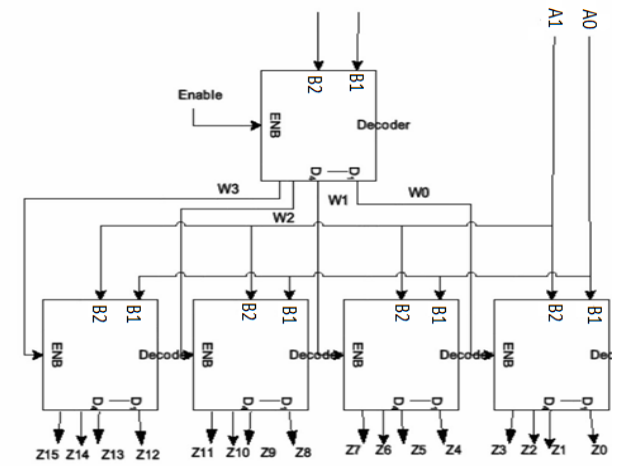

Figure 1: Tree decoder

FPGA based Tree Decoder

The FPGA board Spartan 3E (3s500efg320-5) used to implement the tree decoder has only 8 LEDs to display the output of logic program burnt on it. So, only 8 outputs can be shown at a time on Spartan 3E. This limitation of FPGA board is removed by a new logic encoded in the previous described tree decoder. The logic employed to show 16 output lines in two sets of 8 output lines each is presented next. As we have to map 16 outputs onto 8 outputs of LEDs, we require one more enable input which works in such a way that it selects higher order 8 outputs if it is logic 1 and selects the lower order 8 outputs when it is logic 0. The function thus implemented can be given asfollows:

This structure of tree decoder consists of following parameters. 4 inputs given as: A0, A1, A2, X3
2 enable input: en and en1
16 output stages: Z0 , Z1 , Z2 , Z3 , Z4 , Z5 , Z6 , Z7 , Z8 , Z9 , Z10, Z11 , Z12 , Z13 , Z14 , Z15
It is composed of

1. 5 number of 2 to 4decoders.
2. 4 AND gates
3. 8 ORgates

The input to 4 to 16 decoder is divided into two equal halves and each half is named accordingly.
I.e. X = (Xleft +Xright)
Where, Xleft = (X3 ,A2) and Xright = (A1 , A0)

The first 2 to 4 decoder at the top receives the Xleft inputs of Main input and enable as its input lines.
Mathematically,
W = Dec (Xleft, en)
Where W = W0, W1, W2, W3 are the four outputs of 2 to 4 Decoder DEC.

The output lines of this top decoder are fed to four different AND gates. The second input to AND gates are from en1 input. The output of these AND gates become the enable input for below decoders at level 2.The two AND gates which works as enable input for higher 8 bit outputs is fed directly with en1 input while there is two AND gates which work as enable for lower

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8bit outputs is fed through the complement of en1. The inputs to level 2 decoders are the Xright part of main input. Lastly, to map 16 outputs for two sets of 8outputs each, the corresponding bits of higher 8outputs are Red with corresponding bits of lower 8 outputs. Thus the circuit is implemented.

When en1 = 0, Z shows lower 8 bits of output for given input combination and en1 = 1, Z shows higher 8 bits of output for given input.

Thus,

Z = fucn {en1, Dec ((Xright , W0) , (Xright , W1) , (Xright, W2), (Xright, W3))}

Where, Z is the combined output of level 2 decoders' i.e. DEC0, DEC1, DEC2 and DEC3.

IV. SIMULATION & SYNTHESIS

RTL Schematic

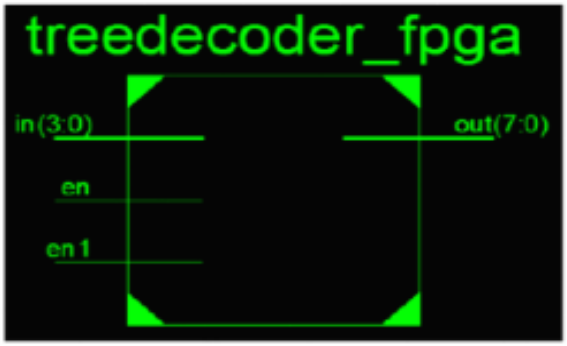

Figure 2: Tree decoder using FPGA

Detailed Schematic

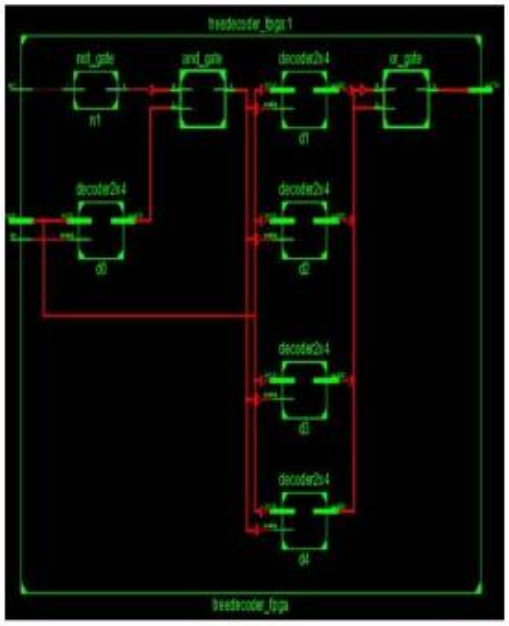

Figure 3: Schematic diagram for tree decoder

Table I
Parameter Utilization

Parameter	% Utilization
Number of slices	08
Number of 4 input LUTs	22
Number of IOBs	20
Maximum delay	6.246ns
Total memory usage	1984113

V. CONCLUSION

From the above results we conclude that the decoder designed and implemented by symmetric tree decoder method requires much less utilization of components. Thus requires much less memory space for fabrication, low energy for working and comparatively less delay. Apart from these parameters, the circuit structure for a tree decoder is symmetric and regular. Tree decoders are formed of similar sub-modules, thus respects the modularity and regularity ideas of VLSI fabrication requirements. These structures can be modeled by means of normal blocks which are easily available in cell libraries and requirement of solely similar blocks of circuits additionally easies the process of layout designing and fabrication

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